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Noise analysis for switched-capacitor circuitry

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ABSTRACT

Track and hold circuits play a key role in mixed-signal, analog to digital interfaces. They are often used as part of the analog to digital conversion (ADC) process whereby a time-varying analog signal is sampled at the transition of a clock signal and subsequently held for a part of the conversion process. This approach is used, in part, because the remainder of the ADC conversion process is adversely affected if the input signal varies during the conversion.

Noise, and in particular thermal noise, is recognized as a major bottleneck limiting the performance of switched-capacitor circuits and it is essential that all of the major contributors to noise are appropriately considered when designing any switched-capacitor circuit. Invariably, switched-capacitor (SC) circuit designers only discuss noise generated in the track mode when reporting noise performance and correspondingly ignore noise generated in the hold mode. In particular, most authors simply use the well-known expression kT/C to represent the variance of sampled thermal noise present on a sampling capacitor[16]-[19]. The spectrum of the continuous-time sample and hold noise has been discussed as the switches capacitor circuitry field evolved [1]-[3] but the early authors didn't discuss the relationship between the spectrum of the sample and hold noise and the sampled noise characterized with the kT/C expression. More important, noise present during the hold mode which affects subsequent sampling has not been discussed in the literature. In the thesis, the continuous noise which is generated during the second phase of a SC circuit will be compared to the S/H noise.

In chapter two of this thesis, a numerical comparison between the RMS value of the continuous-time S/H noise and the sampled kT/C noise is presented. In chapter three, thermal noise present during the hold mode for two switched-capacitor circuits which are often used

in analog to digital converters are investigated and compared with the standard sampled noise expression. In chapter four, it is shown that when these switched-capacitor circuits are used in an analog to digital converter with low speed and small resolution, the continuous-time hold noise can be justifiably neglected but when the sample frequency and resolution get higher, the noise that is generated in the hold phase is not negligible and can cause significant performance degradation of the system.

CHAPTER 1 OVERVIEW

The class of analog circuits using periodic sampling techniques is called analog sampled data circuits. In this chapter, author will introduce the background, development and problem of this type of circuits, especially noise in these sampled data circuits.

1.1 Introduction

Nowadays, sampled data circuits are widely used in integrated mixed signal systems. Such functions include switched-capacitor filters, analog to digital converters and so on.

The sampling of analog signals was discussed as early as the 1870's when James Clark Maxwell developed the fundamental theory of sampled data circuits—the equivalent resistance of a periodic switched-capacitor which is shown in equation (1.1) [4] and will be explained in detail in a later section of this chapter.

$$R = \frac{T_c}{kC} \tag{1.1}$$

During the late 1950s and early 1960s, the theory of sampled data circuits evolved [5]. However, they were not used widely until semiconductor technology was developed so that switches could be embedded into integrated circuits. In particular, Hodges and Gray of Berkeley and Brodersen/Copeland [26][27] found switches can be practically realized with MOSFETS[6]-[13]. From then on, sampled data circuits or switched-capacitor circuits by using MOSFETS as switches have been widely used in analog design.

1.2 Resistance of Switched-capacitor circuits

In continuous-time analog circuits, capacitors, resistors and active components, especially the previous two, determine the performance of the entire circuits. However, it is at high cost or even impossible to accurately control these components due to inherent variations in process and environment.

Let us take a filter as an example. Resistors and capacitors must be accurately defined to meet stringent specifications such as bandwidth, center frequency or quality factor. However, because of process variations alone, variations of the value of integrated resistors and capacitors can be as large as 30%. This causes a serious problem in filter design where effective RC products often must be accurate to well under 1%. Another problem is that, if the center frequency of the filter is relatively low, it requires a large value for resistors and this in turn requires large area.

After MOSFETs were available, some attempted to use MOSFETs as resistors. However, the nonlinear dependence of the resistors on the gate to source and drain to source voltage made the circuits highly nonlinear.

Switched-capacitor circuits are able to jointly minimize the concerns about large variability in component values and large area required for low frequency system poles. . Additionally, switched-capacitor circuits usually relax the requirement of bandwidth of the Op Amp compared to what is required in comparable continuous-time circuits.

1.2.1 Derivation of Resistance of SC Circuits

It is well-known that the switched-capacitor of Figure 1 and the resistor of Figure 2 can be essentially equivalent if the clock frequency of the complimentary non-overlapping clocks Φ_1 and Φ_2, of Figure 3, is high.

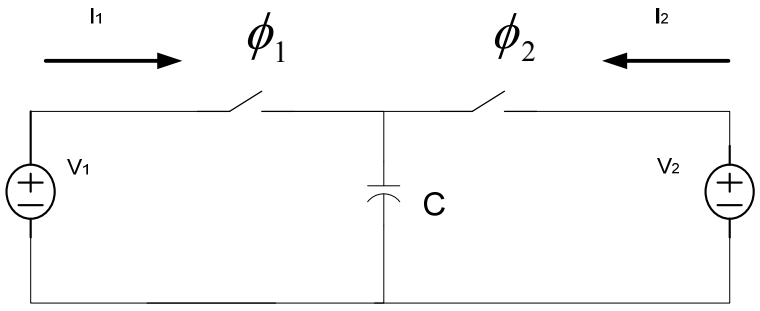


Figure 1. Switched-capacitor circuit

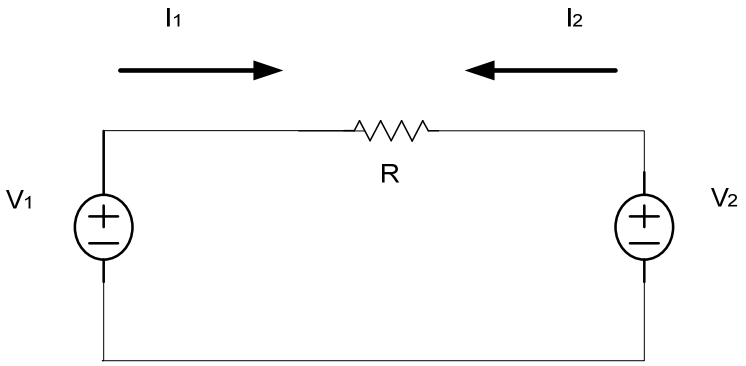


Figure 2. Equivalent resistor circuit

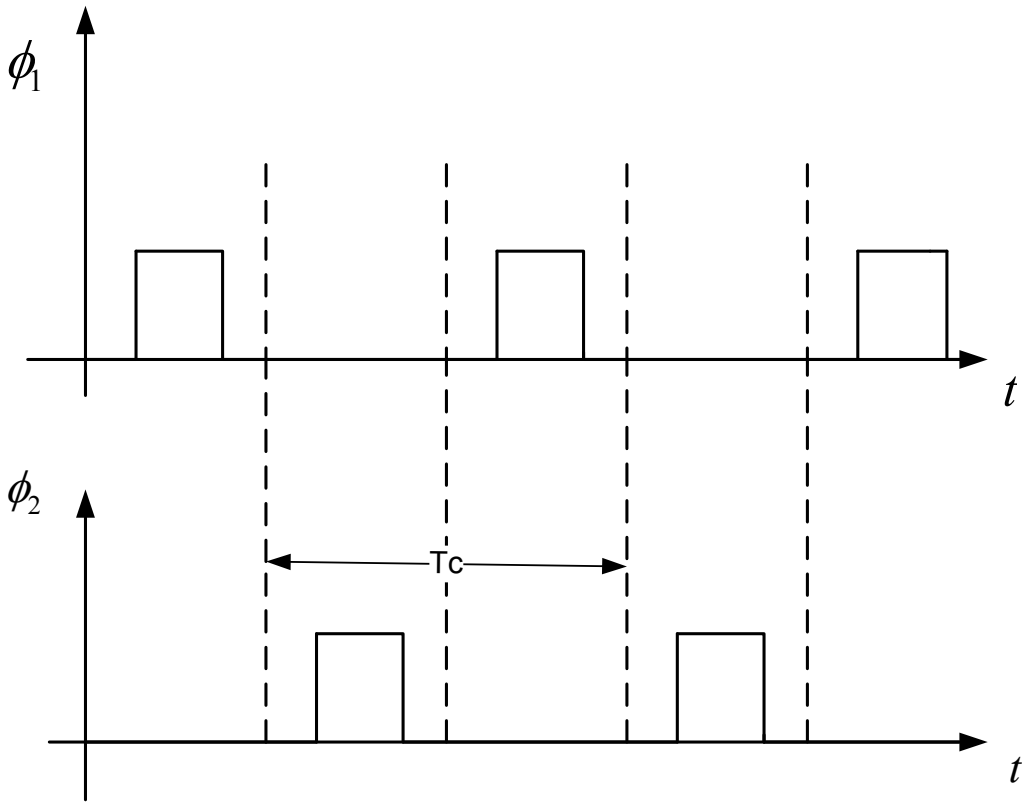


Figure 3. Clock waveforms for the switched-capacitor circuits

The current carried by the resistor R in Figure 2 is given by $I=(V_1-V_2)/R$.

In Figure 1, the average current flow from V_1 to V_2 is the ratio of the transferred charge to the clock period T_c as given by in one clock period

$$I_{12} = \frac{C_s\left(V_1 - V_2\right)}{T_c} = C_s f_c\left(V_1 - V_2\right) \tag{1.2}$$

Comparing (1.1) and (1.2), if flows that we can view the switched-capacitor as being equal to a resistor of value $(C_S f_c)^{-1}$. The circuit of Figure 1 is not a stray insensitive circuit. Parasitic capacitors will seriously affect the accuracy of the equivalent resistance value. In the following, several other switches capacitor circuits will be discussed as alternatives through of this thesis.

Another well-known switched-capacitor circuit is shown in Figure 4. It can be easily seen that the equivalent resistor value of this switched-capacitor realization is:

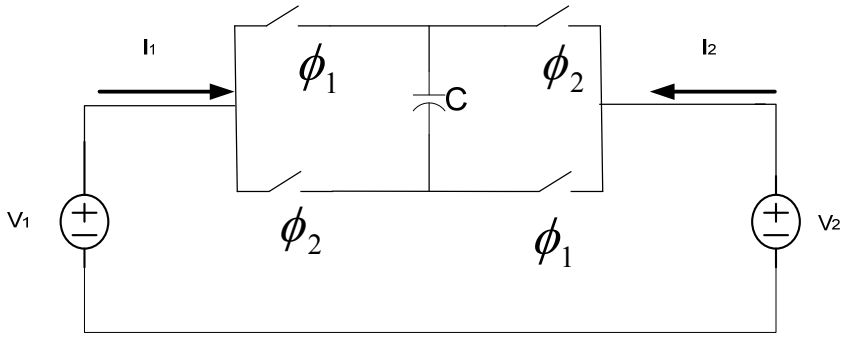


Figure 4. Bilinear switched-capacitor realization of a resistor

$$R = \frac{T_c}{4C} \tag{1.3}$$

There are many other realizations of a resistor by using switched-capacitor circuits. It can even realize a negative resistor as well. So the general expression for the resistor equivalence of a switched-capacitor circuit can be written as:

$$R = \frac{T_c}{mC} \tag{1.4}$$

1.2.2 The Advantage of SC Circuits as a Resistor

The well-known benefits that can be derived from SC circuitry can be seen by considering the integrator as an example. One of the simplest integrators is shown in Figure 5.

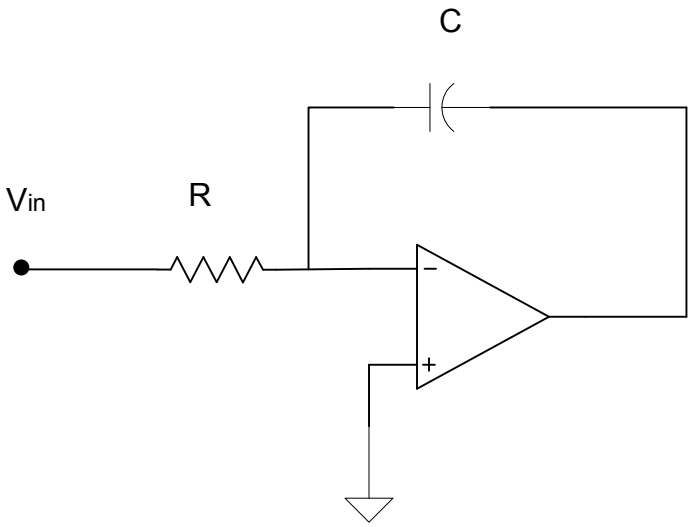


Figure 5. Integrator

$$V_{out} = -\frac{1}{RC}\int V_{in}dt \qquad (1.5)$$

The unity gain frequency is 1/RC. It depends on the absolute value of R and C. Due to process variation, integrated R and C component can vary by ±30% which is usually not tolerable in analog circuits.

According to the forgoing theory in section 1.2, we can replace the resistor R by a switched-capacitor circuit. The switches can be realized by MOSFETS such as shown in Figure 6.

The output of the circuit can be obtained by replacing R in equation (1.5) by $1/(fC_{in})$. We can qualitatively analyze the circuit from another point of view. When Φ_1 is closed, C_{in} will be charged up by V_{in} if given enough time. When Φ_1 is opened and Φ_2 is closed, the charge on C_{in} will be dumped on to C_F. During the next period of operation, another charge from V_{in} will be dumped onto C_F, resulting in an integration at the output.

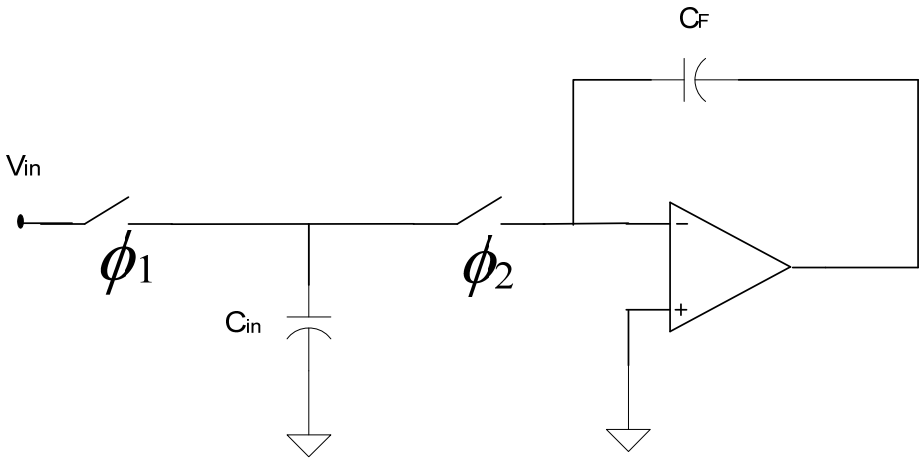


Figure 6. Switched-capacitor integrator

The unit gain frequency of the circuit shown in Figure 6 is fcC_{in}/C_F. This is equal to the ratio of the capacitors and a clock frequency. This can be accurate up to 0.1%. The switched-capacitor circuits improve the accuracy by around 300 times compared to what is achievable with a continuous-time RC integrator.

Additionally, after Φ_1 is opened and Φ_2 is closed, the charge on C_{in} suddenly imparts a voltage at the null port of the Op Amp, causing the Op Amp to slew. So instead of operating in the linear region, the Op Amp will slew and the output will increase at the slew rate and then settle exponentially. With the large over-drive at the null-port of the Op Amp, the time required for the output of the Op Amp to reach the final valued decreases as to that required for the continuous-time RC integrator, thus relax the bandwidth requirement of the Op Amp.

Amplifier with resistive feedback can be realized by switched-capacitors as well by using the same methods. For example the flip-around gain stage and the charge-redistribution gain stage.

However, the switched-capacitor has several issues. In the following section, author will talk about problems exist in switched-capacitor circuits.

1.2.3 Issues in a SC Circuits

1.2.3.1 Channel charge injection in switched-capacitor circuits

When the MOSFET is "on", charge will be stored on the channel capacitor. After the switch is turned off, the charge has to be dumped somewhere. It is not easy to determine how much charge will be dumped onto C_L and how much will be dumped back to V_{IN}. The way the charge is split depends on the magnitude of the clock signal, and magnitude of input signal, the wave shape of the clock signal and the impedance seen at both the drain and source of the switch. If it is an input dependent split, it will cause gain error, dc offset and nonlinearity in the SC integrated (shown in Figure 6) or in a SC filter.

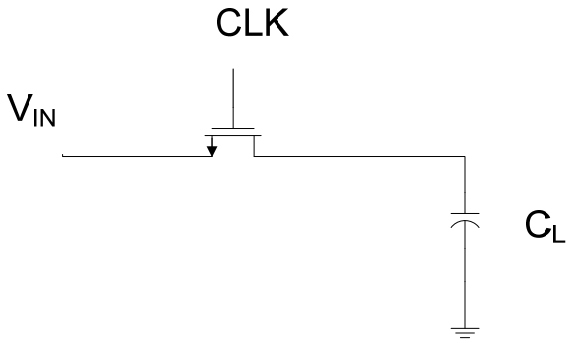


Figure 7. Channel charge distribution

Channel charge injection can be eliminated by sequentially turning on and off switches. For example, in Figure 8, the input dependent channel charge injection will affect the charge on C_1 at the end of Φ_1, and during Φ_2 when the charge on C_1 is dumped onto C_2, and cause gain error and nonlinearity of the circuit. If the M_3 is turned off earlier than M_1, than when M_1 is turning off, the right node of C_1 is floating and there is no way to charge C_1 up. Hence all the channel charge of M_1 will go to V_{IN}, making the circuit input independent. For more explanation, please refer to [14].

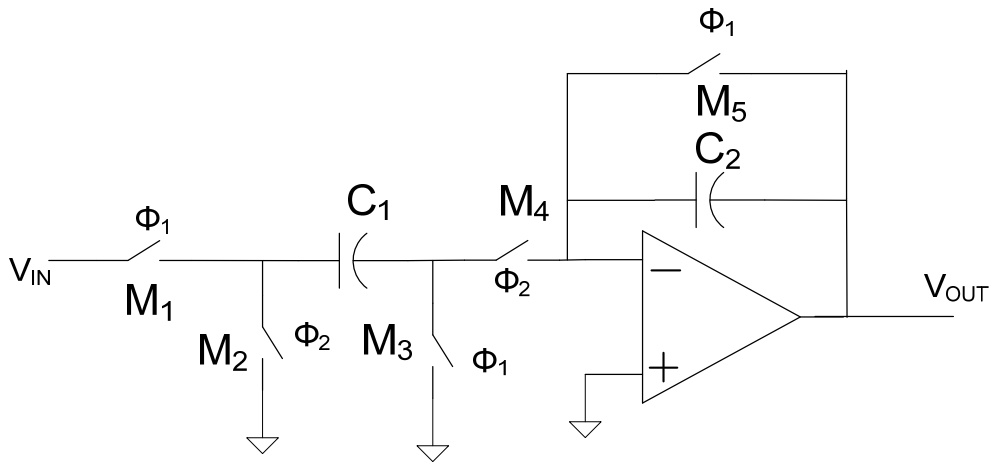


Figure 8. Charge-redistribution gain stage

1.2.3.2 Clock feed through

Clock feed through is another issue of SC circuits.

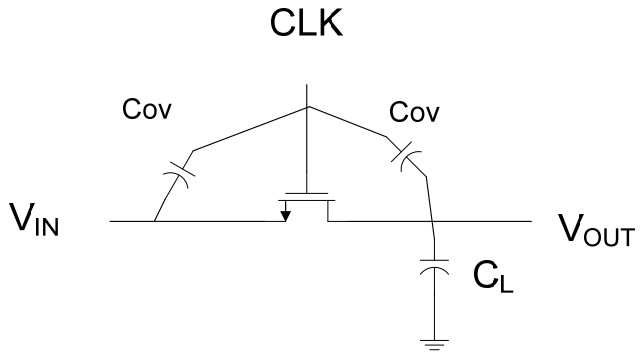


Figure 9. Clock feed through in SC circuit

There is an overlap capacitor between the gate-source and gate-drain of the MOSFET, forming a voltage divider between the CLK signal and V_{OUT}. Assuming the input is grounded, there will be an error voltage at V_{OUT} which can be written as

$$\Delta V = V_{CK} \frac{WC_{ov}}{WC_{ov} + C_H} \tag{1.6}$$

Although there is an error voltage at the output, it is a constant value and can be regard as a constant offset voltage. Hence if it causes a problem in a given application, it can be eliminated by offset cancellation techniques.

1.2.3.3 Thermal noise

Thermal noise is another issue of SC circuits and has become the bottleneck of using the SC circuits to achieve high resolution and high speed. The effects of thermal noise will be reviewed in this section. Take a 1st order SC circuit as an example as shown in Figure 10. When the switch is turned on in the first phase, it can be modeled as a resistor R as shown in Figure 10 (b). This is termed the track mode or sample mode of the sampling circuit. When the CLK is off in phase 2, it can be modeled by an open circuit as shown in Figure 10 (c). This is termed the hold mode of the sampling circuit.

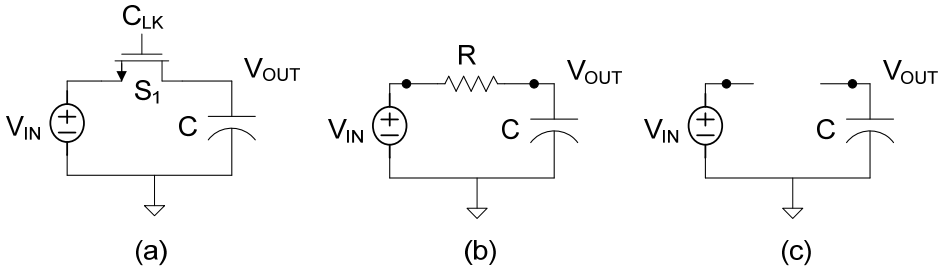
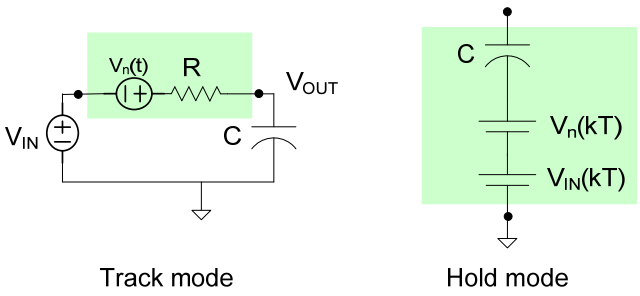


Figure 10. Single-transistor sampler a) transistor implementation of switch, b) track mode, c) hold mode

Consider again the track and hold amplifier of Figure 10, during the track mode, the MOSFET is operating in the triode region and behaves as a resistor. During the hold mode, it acts as an open circuit. Any resistor, including the MOSFET when acting as a resistor in the track mode, is noisy and the dominant noise is often the thermal noise that is due to the random movement of electrons in the resistor. This can be modeled as a series noise voltage source as shown in Figure 11 (a). When the switch opens, the capacitor voltage is ideally $V_{IN}(kT)$, where T is the clock period and where it is assumed that the phase of the clock is such that time kT is near the end of the hold interval of the kth clock period. The actual voltage on the capacitor will differ from the ideal value by a noise voltage $V_n(kT)$ due to the thermal noise coming from the switch resistance that was present during the track mode. The clock phasing is shown in Figure 12. The noise voltage $V_n(kT)$ is a noise sequence.



(a) (b)

Figure 11. Equivalent Circuit of Sampler in a) Track Mode b) Hold Mode

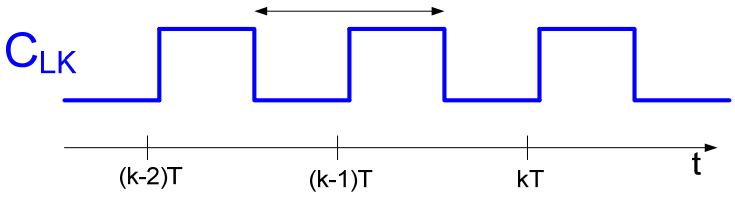


Figure 12. Timing Diagram of Sampling Clock

The noise power spectral density of a resistor R is equal to

$$S_R = 4kTR \tag{1.7}$$

The transfer function from input to output is

$$H(jw) = \frac{1}{1 + jwRC} \tag{1.8}$$

The noise voltage on the capacitor during the track mode has noise spectral density

$$S_{VOUT} = 4\mathrm{kTR}\left(\frac{1}{1+(\mathrm{RC}\omega)^2}\right) \tag{1.9}$$

where $\omega=2\pi f$. The RMS noise voltage on the capacitor is given by

$$V_{n_{RMS}} = \sqrt{\int_{f=0}^{\infty} S_{VOUT}\,df} = \sqrt{\int_{f=0}^{\infty} \frac{4\mathrm{kTR}}{1+\omega^2R^2C^2}\,df} \tag{1.10}$$

But, recall the definite integral

$$\int_{y=0}^{\infty} \frac{1}{1+y^2}\,dy = \left(\tan^{-1} y\right)\Big|_{y=0}^{\infty} = \frac{\pi}{2} \tag{1.11}$$

It follows from a change of variables and this definite integral that

$$V_{n_{RMS}} = \sqrt{\int_{f=0}^{\infty} S_{V_{OUT}}\,df} = \sqrt{\frac{kT}{C}} \tag{1.12}$$

Note this is independent of the size of the resistor R. This is because the noise spectral density within the bandwidth of the RC filter is proportional to R but the bandwidth is inversely proportional to R. So the total noise power is independent of R. This is often referred to the "kT/C" noise associated with a capacitive sampler. As an example, it thus follows that the RMS noise voltage sampled on a 1pF capacitor is 64.4μV. This analysis was undertaken in the continuous-time domain. To a sample and hold circuit, operation is done discretely, so in the next chapter, a discussion about the relationship between the discrete noise and continuous noise domains will be given.

From equation (1.12), we find that the noise depends only on the value of capacitor. To reduce the thermal noise of the SC circuit, we have to increase the size of capacitor. However, this will decrease the speed of the circuit or increase the power consumption. Hence, the thermal voltage becomes a bottleneck of today's high performance SC circuits.

1.3 Conclusion

In this chapter, we have briefly reviewed the history of switched-capacitor circuits. We have discussed the advantages and disadvantages of the SC circuits. The ratio of capacitors determines the accuracy of key characteristic of the circuits; for example the unity gain frequency of integrator. Hence, switched-capacitor circuits can improve accuracy compared to what is achieved with continuous-time circuits. It relaxes bandwidth requirement of Op Amp as well. However, SC circuits have input dependent channel charge injection, causing gain error, dc offset and nonlinearity to the circuits. And the overlap

capacitors between the gate and diffusion of MOSFETs cause clock feed through and an error voltage will appear at output node. However, these issues can be eliminated by sequentially turning on and off switches and offset cancellation methods. The other issue of the SC circuits is the thermal noise from the resistance of switches. The RMS value is inversely proportionally to the value of capacitors and independent of resistors. And thermal noise becomes the bottleneck of the high performance circuits nowadays.

CHAPTER 2 NOISE ANALYSIS FOR BASIC SC CIRCUITRY

As stated in the chapter 1, for switched-capacitor networks, people usually use $\sqrt{kT/C}$ to express the thermal noise voltage contributed by switched-capacitors. This equation is valid under the assumption that the bandwidth of thermal noise is much larger than the clock frequency, in other words, it is an oversampling circuit. However, the cut off frequency of the thermal noise in most cases exceed sampling rate by orders of magnitude. This results in an undersampling of the wideband noise components and aliasing of the high frequency back into low frequency. In this part, it will show that the RMS value or the power of the thermal noise calculated from the accurate spectrum analysis has the same order of magnitude of that from kT/C analysis. The accurate analysis will be discussed in this chapter.

2.1 Noise PSD Analysis for SC Circuits

In this section, the analysis and derivation will be given first to the 1st order (one pole) switched-capacitor low pass filter. The PSD analysis will be extended to two SC gain stages in the next chapter.

2.1.1 Some Useful Theorem

Some well-known theorems that relate noise of a sampled signal to noise in a continuous signal are quite useful in relating noise in the continuous-time domain to the corresponding noise in the discrete-time domain. Four useful theorems will now be reviewed. Assume V(t) is a continuous-time zero-mean noise signal (with appropriate stationary properties) and that the sequence <V(kT)> is a sampled version of V(t) sampled at times T, 2T, …

The RMS value of V(T) is defined to be

$$V_{RMS} = E\left(\sqrt{\lim_{T\to\infty}\left(\frac{1}{T}\int_0^T V^2(t)dt\right)}\right) \tag{2.1}$$

And the RMS value of the sequence <V(kT)> is defined to be

$$\hat{V}_{RMS} = E\left(\sqrt{\lim_{N\to\infty}\left(\frac{1}{N}\sum_{k=1}^{N} V^2(kT)\right)}\right) \tag{2.2}$$

where the operator E is the expected value operator.

Theorem 1 If V(t) is a continuous-time zero-mean noise source and <V(kT)> is a sampled version of V(t) sampled at times T, 2T, …., then the RMS value of the continuous-time waveform is the same as that of the sampled version of the waveform. This can be expressed as

$$V_{RMS} = \hat{V}_{RMS} \tag{2.3}$$

Theorem 2 If V(t) is a continuous-time zero-mean noise source and <V(kT)> is a sampled version of V(t) sampled at times T, 2T, ….,then the standard deviation of the random variable V(kT), denoted as $\sigma_{\hat{V}}$ satisfies the expression

$$\sigma_{\hat{V}} = V_{RMS} = \hat{V}_{RMS} \tag{2.4}$$

Note: There are some parts of the hypothesis of these two theorems that have not been stated such as stationarity of the distribution and no correlation between samples spaced T seconds apart. Part of this theorem appears in [21].

Theorem 3 If V(t) is a continuous-time zero-mean noise source with power spectral density S_V, then the RMS value of the noise is given by

$$V_{RMS} = \sqrt{\int_{f=0}^{\infty} S_{V^{df}}} \tag{2.5}$$

Theorem 4 The RMS value and the standard deviation of the noise voltage that occurs in the basic switched-capacitor sampler (Figure 15) is related to the capacitor value by the expression

$$V_{RMS} = \sigma_{\hat{V}} = \sqrt{\frac{kT}{C}} \tag{2.6}$$

This theorem follows from Theorem 2 and Theorem 3. The derivation for the RMS value of the sampled noise voltage was derived previously.

As stated before, Theorem 2 will only be true when the samples are not correlated. However, as the track-mode circuit is actually a filter, there will be some correlation between the samples in most cases. So in the following chapter, another method PSD analysis will be used to calculate the RMS value of the sampled noise and will be compared to the kT/C analysis.

2.1.2 Power Spectral Density (PSD)

The frequency content of a signal is a very basic characteristic that distinguishes one signal from another. In general, a signal can be classified either as a finite (nonzero) average power (infinite energy) signal or as a finite energy (zero average power). The frequency domain expression of a finite energy signal can be obtained by Fourier transform of the corresponding time domain function.

A non-zero stationary stochastic process is an infinite energy signal and hence its Fourier transform does not exist. The spectral characteristic of a stochastic signal is obtained by computing the Fourier transform of the autocorrelation function. i.e. the power spectral density (PSD) [20].

Consider a linear time-invariant system (filter) that is characterized by its impulse response h(t) whose frequency response is H(f). Let x(t) be the input signal to the system and let $y(t)$ be the output signal. The output of the system can be express as

$$y(t) = \int_{-\infty}^{\infty} h(\tau)\, x(t-\tau) d\tau \tag{2.7}$$

The power density spectrum of the output signal can be express in the form of

$$S_y(f) = S_x(f)\left|H(f)\right|^2 \tag{2.8}$$

where $S_y(f)$ is the power spectral density of the output signal and $S_x(f)$ is the power density spectrum of the input signal.

As the Theorem 3 says in previous section, if V(t) is a continuous-time zero-mean noise source with single-side power spectral density S_V, then the RMS value of the noise is given by

$$V_{RMS} = \sqrt{\int_{f=0}^{\infty} S_{V^{df}}} \tag{2.9}$$

2.1.3 Noise PSD of Continuous-time Circuits

The noise power spectral density of the output of the 1st order RC low pass filter (Figure 13) can be approximated by the rectangular region shown in line in Figure 14. The effective noise bandwidth is: [1]

$$f_{eff} = \frac{1}{4RC} = \frac{\omega_{3dB}}{4} \tag{2.10}$$

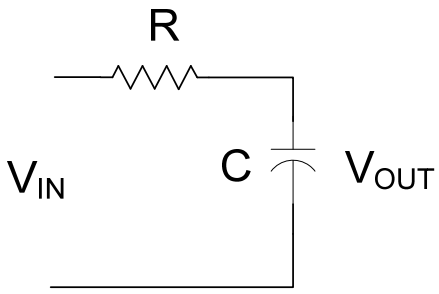


Figure 13. First order low pass filter

2.1.4 PSD of Sampled Noise

We will now allow the switch to operate that in the sampling period T_c, where it is closed for αT_c, and opened for $(1-\alpha)T_c$. Here α is the duty cycle as shown in Figure 16.

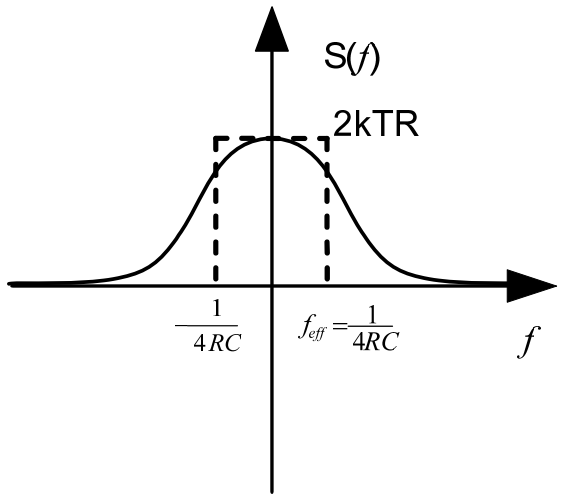


Figure 14. Noise power spectral density

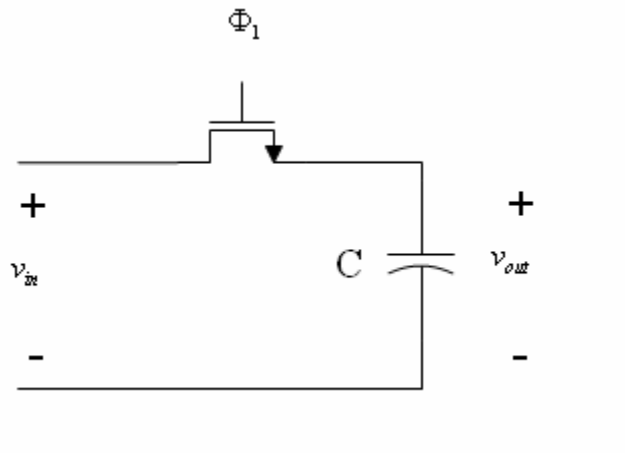


Figure 15. First order switched-capacitor low pass filter

The continuous-time output of an ideal track and hold sampler is shown in Figure 17 where the sample is taken on the falling edges of the clock. In many applications, only the sampled output near the end of the hold interval is of interest. The sampled values near the end of the hold period are shown in Figure 18. In this situation, the sampled waveform can be thought of as a discrete-time rather than a continuous-time waveform and it can be represented as a sequence $V_{OUT}(kT)$ where T is the period of the sampling clock. The reference to the clock period, T, can be suppressed and the sampled output can simply be though of as a sequence of real numbers as suggested by the sequence in Figure 18.

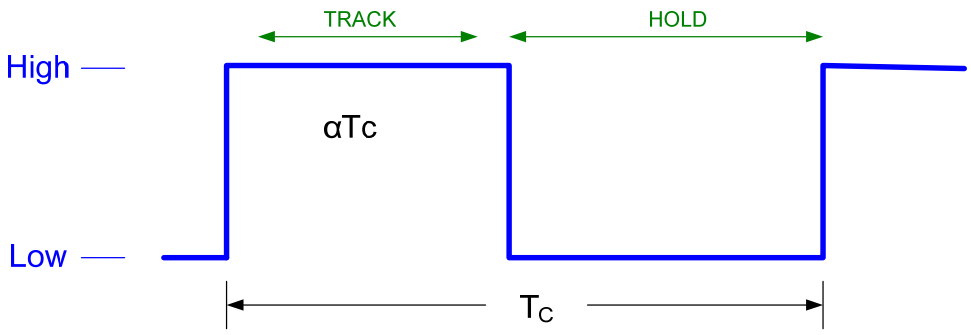


Figure 16. Timing diagram for sampler circuit

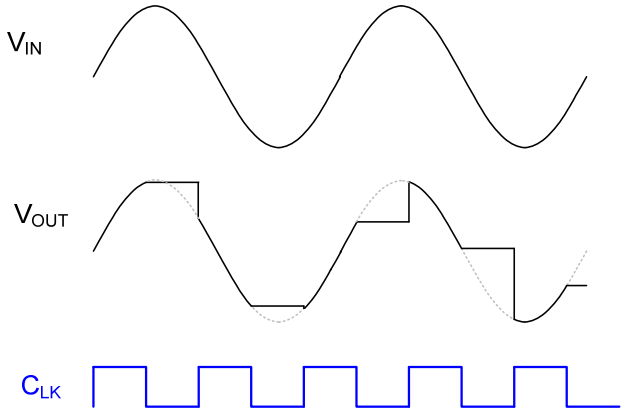


Figure 17. Continuous-time track and hold operation

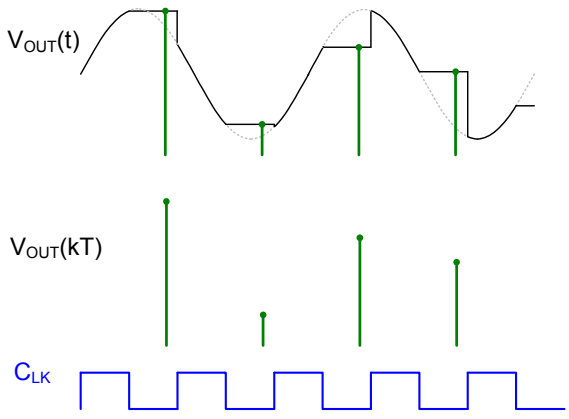


Figure 18. Discrete-time sampled sequence

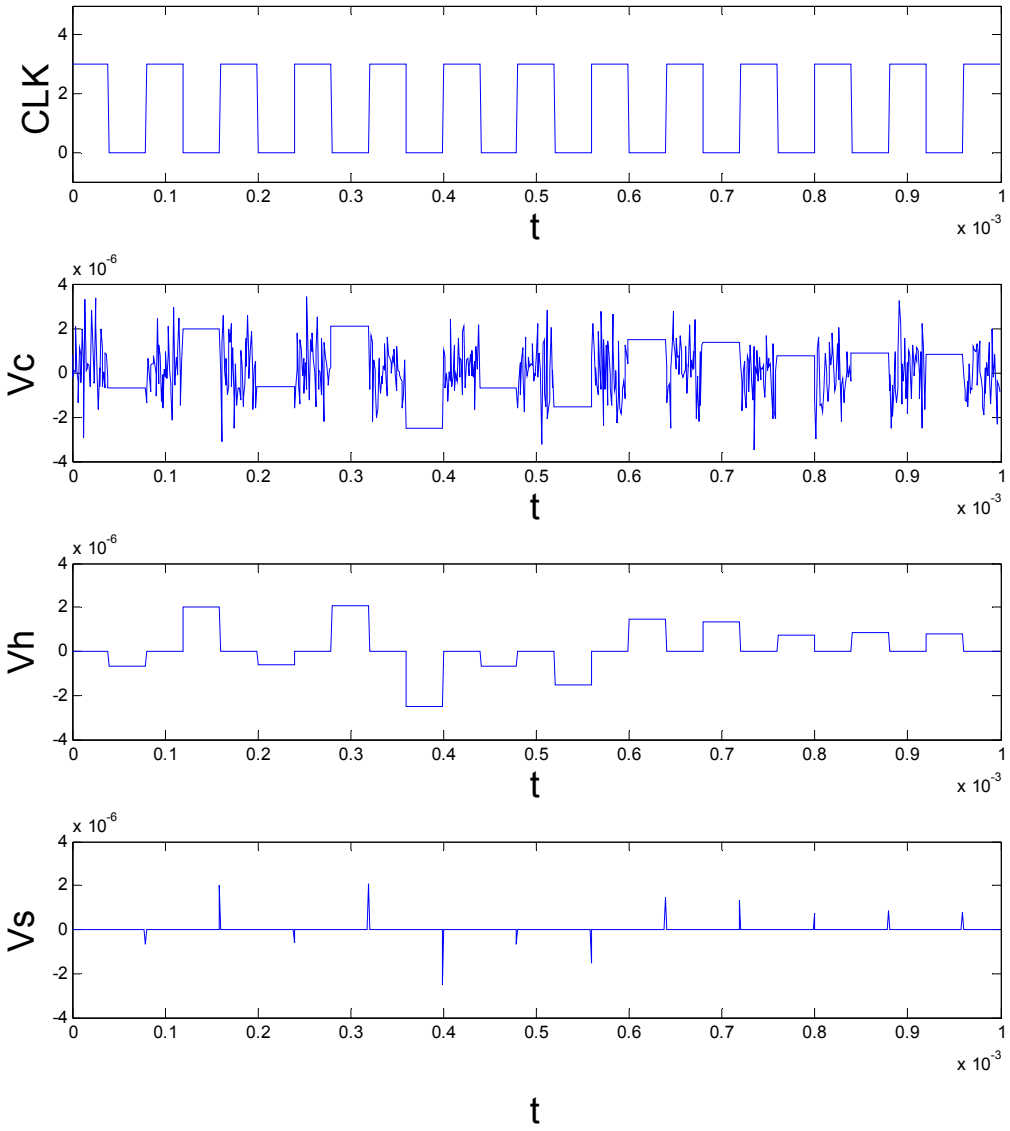


Figure 19. Sampled and hold noise

The noise on the sampled output looks like the waveform in Figure 19, where V_C is the total noise. V_t is the noise in track phase. V_h is the noise in hold phase. Conceptually, it is constructed by sampling V_t at the end of track phase and then holding that value to the end of

the hold phase. The sequence Vs is constructed from sampling V_h at the end of hold phase. The relationship between V_C, V_t and V_h is given by the equation $V_c = V_t + V_h$.

The single-sided PSD of V_t is given by

$$S_t(f) = \frac{4\alpha kTR}{1+(2\pi RCf)^2} \tag{2.11}$$

and the corresponding RMS value of V_t is given by

$$\overline{v_t^2} = \frac{\alpha kT}{C} \tag{2.12}$$

2.1.4.1 PSD of sampled noise V_s

If the noise is highly undersampled at the output of a low pass filter, i.e. the sampling frequency is much smaller than the noise bandwidth, aliasing from high frequencies to low frequency will occur. This is shown in Figure 20. The frequency response must be shifted by integer multiples of $f_c = \frac{1}{T_c}$ where *f*c is the sampling frequency. So the spectral density in the base-band, that is for $-fc/2 \le f \le fc/2$, becomes:

$$S_s(f) = \sum_{k=-\infty}^{k=\infty} S_{RC}(f - kf_c) \tag{2.13}$$

where S_{RC} is the two-sided PSD of the continuous-time noise.

There are approximately N aliased two-sided spectrums in the bandwidth from 0 to $\frac{f_c}{2}$ where

$$N = 2\frac{f_{eff}}{f_c} = \frac{1}{2RCf_c} \tag{2.14}$$

Thus, since the power spectral density S_{RC} is approximately constant, the spectrum $S_S(f)$ is also constant and proportional to the effective bandwidth of the noise.

If $f_{eff} >> f_c$ (e.g. $f_{eff} > 5f_c$), then the PSD of sampled noise is [2]:

$$S_{RC}(f) = \begin{cases} S_{RC0} & -f_{eff} \le f \le f_{eff} \\ 0 & elsewhere \end{cases} \tag{2.15}$$

here S_{RC0} is the two-sided PSD of the continuous noise at zero frequency.

Up to this point, emphasis has been placed upon characterizing the continuous-time noise in the SC network which is comprised of a track phase noise, v_t and a hold phase noise, v_h. The sampled hold phase noise, v_s in Figure 19 is actually discrete-time sequence. This can be viewed as a continuous-time noise source as well, $V_{SAM}(t)$, by passing v_s to a zero-order sample and hold. $V_{SAM}(t)$ can be thought of as a modified version of $v_h(t)$ where the hold period is stretched to T_{CLK} or, equivalently, where α in Figure 16 is set equal to 1. The spectrum of $V_{SAM}(t)$ can be obtained from that of $v_n(t)$ by dividing by α. The two-side thermal noise is characterized by $S_{RC0}=2kTR$. Hence the two-sided sample noise spectrum becomes:

$$S_{SAM}(f)=\sum_{i=-N/2}^{i=N/2-1} 2kTR = 2kTRN = \frac{2kTR}{2RCf_c} = \frac{kT}{Cf_c} \tag{2.16}$$

The total RMS noise can be obtained by integrating $S_{SAM}(f)$ over the base-band $[-f_c/2, f_c/2]$. Thus, the integrated sampled noise becomes:

$$\overline{v_s}^2 = \int_{-f_c/2}^{f_c/2} S_s(f)df = \frac{kT}{C} \tag{2.17}$$

So the total noise power of $V_{SAM}(t)$ or variance in the base-band $-\frac{f_c}{2} \le f \le \frac{f_c}{2}$ due to all replicas is simply kT/C. The aliasing due to the sampling of the noise thus concentrates the full noise power of the switch resistor into the base-band.

The total noise power in the base-band is independent of R because although reducing R can reduce direct thermal noise PSD, it increases the noise bandwidth and thus the aliasing and the two effects cancel.

2.1.4.2 PSD of noise V_h during hold phase

If the sampled noise is held with the duty cycle (1-α)T, then the single-sided PSD becomes [3]:

$$S_{nsh}(f)=(1-\alpha)^2\,\mathrm{sinc}^2\left((1-\alpha)\frac{\pi f}{f_c}\right)\sum_{k=-\infty}^{k=\infty} S_{RC}(f-kf_c) \tag{2.18}$$

where $S_{RC}(f)$ is given by (2.15).

Substituting equation (2.16) into equation (2.18), we get the single-sided PSD:

$$S_{nsh}(f) \cong (1-\alpha)^2 \frac{kT}{f_c C} \operatorname{sinc}^2\left((1-\alpha)\frac{\pi f}{f_c}\right) \tag{2.19}$$

More generally, we can get for all first order circuits:

$$S_{nsh}(f) = (1-\alpha)^2 \frac{w_{3dB}}{f_c} kTR \operatorname{sinc}^2\left((1-\alpha)\frac{\pi f}{f_c}\right) \tag{2.20}$$

where $\omega_{3dB} = 1/RC$, equation (2.20) is the same as the equation (8) in [1].

It is a known fact that as $x \to 0$, $\sin(x) \to x$, and $\sin c(x) \to 1$. Thus, at very low frequencies, i.e. $f \ll f_c$, equation (2.19) can be rewritten as:

$$S_{nsh}(f) \cong (1-\alpha)^2 \frac{kT}{f_c C} \tag{2.21}$$

The RMS value of the noise in the hold phase can be written as:

$$\overline{v}_n = \sqrt{\int_0^\infty S_{nsh}(f)\,df} \tag{2.22}$$

Hence from equation (2.11) and (2.19), the total noise power of the continuous sample and hold noise expressed in terms of the single-sided PSD is

$$S_c(f) = \frac{4\alpha kTR}{1+(2\pi RCf)^2} + (1-\alpha)^2 \frac{kT}{f_c C} \operatorname{sinc}^2\left((1-\alpha)\frac{\pi f}{f_c}\right) \tag{2.23}$$

Integrating (2.23) from 0 to infinity, we can obtain

$$\overline{v}_c^2 = \frac{\alpha kT}{C} + \frac{(1-\alpha)^2}{2(1-\alpha)T_c} 2\frac{kT}{Cf_c} = \frac{kT}{C} \tag{2.24}$$

Thus, the continuous-time RMS noise voltage at the output of the sampler is independent of the duty cycle of the S/H circuit, and has the same RMS value as $V_{SAM}(t)$.

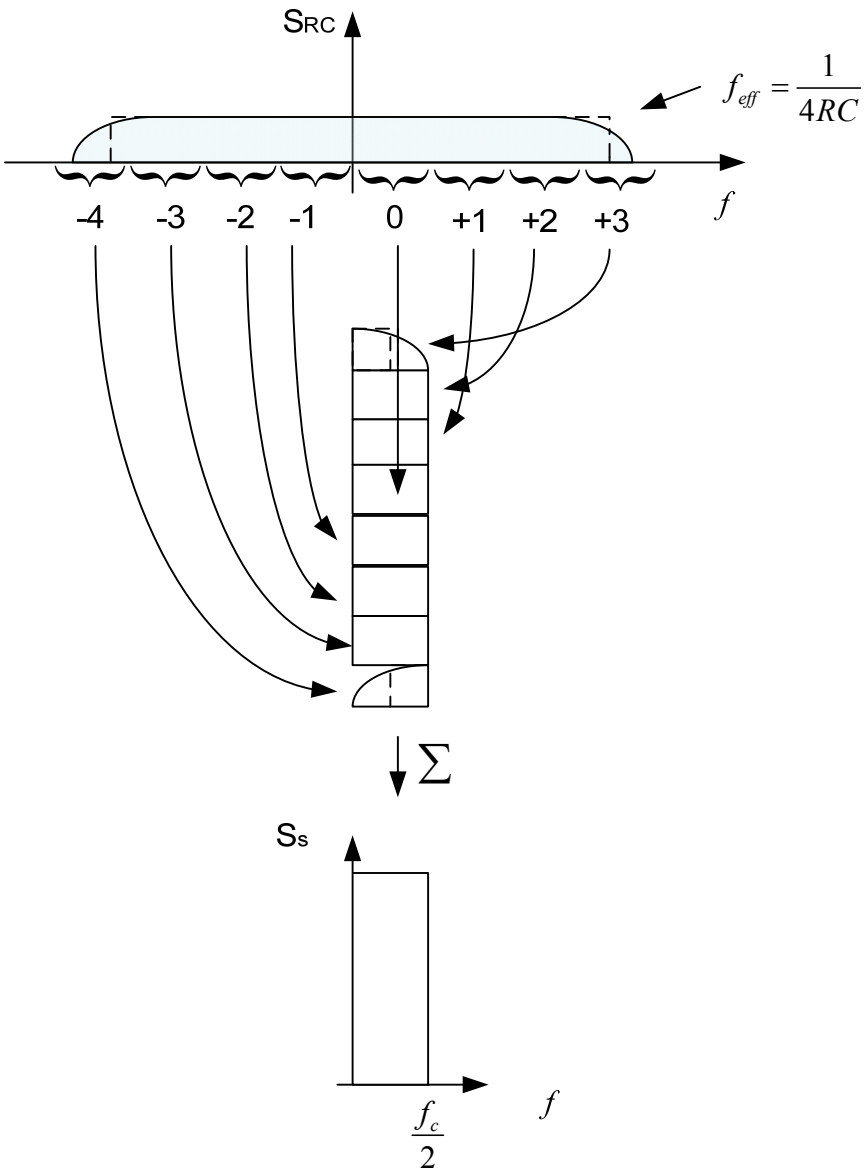


Figure 20. Spectrum of sampled noise

2.1.4.3 Simulation of sampled noise

The derivations in the previous section where often based upon the assumption that the noise spectral in a first-order RC network can be approximated by the dc PSD in the noise bandwidth frequency band with no spectral contributions outside that frequency band. This results in a modest over-estimation of the PSD at the upper end of the noise band and a

modest under-estimation of the PSD outside of the noise band. In this PSD with the Cadence tool SpectreRF are considered and results are compared with those obtained from the theoretical analysis in the previous section.

Consider the first-order SC sampler shown in Figure 21.

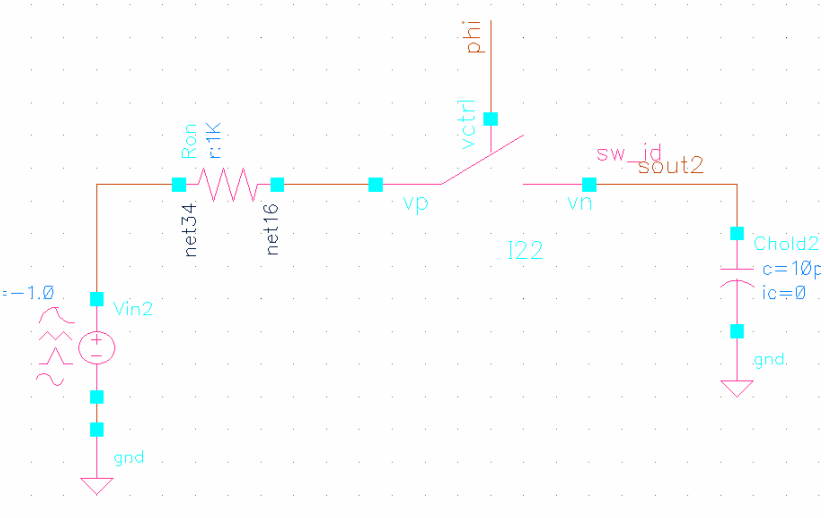


Figure 21. Schematic of the simplest switched-capacitor circuit

The circuit parameters considered in the simulation are listed in Table 1:

Table 1. Simulation parameters

Components	value
R	1kΩ
C	10pF
T_{clk}(Clock period)	2.5μs
α(duty cycle)	0.5

The switch is realized by VerilogA code and it is assumed ideal. A resistor was added in series with the switch to represent the on resistance. In the schematic, it uses a feature that is unique to Spectre-- general voltage source ***vsource.***[15] It can generate ac, dc and so on by

changing the set up of that voltages source. Here in the schematic, only dc source with voltage 0 is used so that this is not voltage source in the schematic.

From equation (2.11) and (2.21), at zero frequency, the total noise PSD is

$$\begin{aligned}\sqrt{S_c(0)} &= \sqrt{S_t(0)+S_h(0)} \\ &= \sqrt{4\alpha kTR + 2(1-\alpha)^2 \frac{kT}{f_c C}}\Bigg|_{\alpha=0.5} \\ &= \sqrt{2kT(1000+62,500)} \\ &= 22.938\text{nV}/\sqrt{Hz}\end{aligned} \tag{2.25}$$

It closely matches the SpectreRF result in Figure 22 .

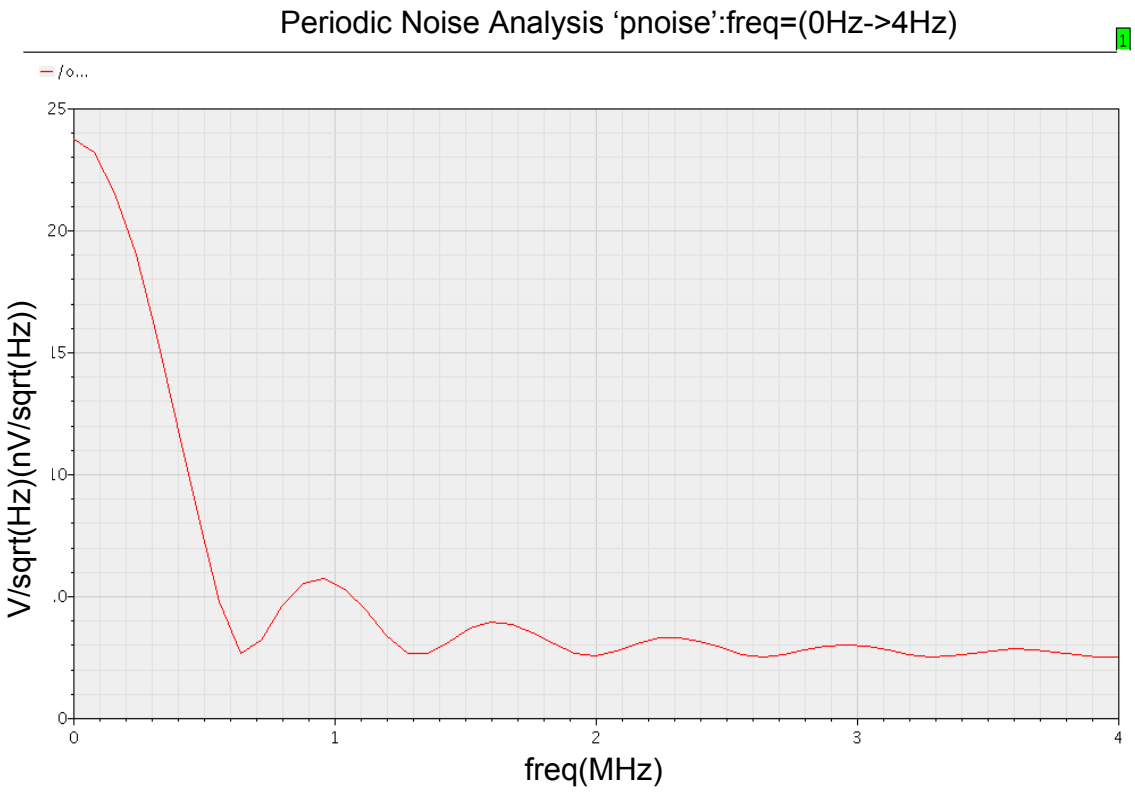


Figure 22. Power spectral density of the total undersampled noise sqrt(S_c)

The PSD of the sampled noise spectrum will now be compared to simulated results. To facilitate this comparison, we will modify equation (2.16) from two-sided spectrum to one-sided spectrum. The single-sided sample noise spectrum becomes:

$$\begin{aligned}\sqrt{S_s(f)} &= \sqrt{\frac{2kT}{f_c C}} \\ &= \sqrt{\frac{2\left(1.381e^{-23}\right)300}{400k\left(10p\right)}} \\ &= 45nV/\sqrt{Hz}\end{aligned} \tag{2.26}$$

The simulation result in Figure 23 is about 39nV/sqrt(Hz). The difference is caused by the limited max frequency SpectreRF can take into account and the small errors associated with assuming the spectral density remains constant throughout the noise bandwidth. If I increase the ***maxacfreq*** parameter, the result will be more accurate and but the simulation time will be increased.

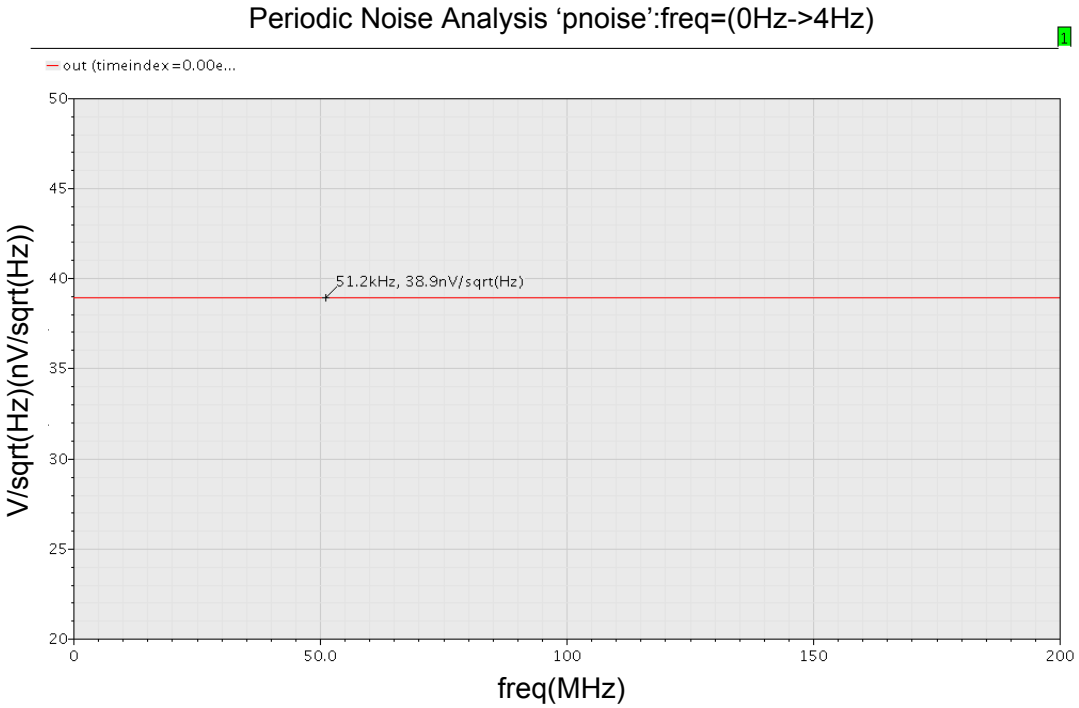


Figure 23. Power spectral density of sampled noise sqrt(Ss)

2.1.5 Conclusion

It has been shown from the foregoing derivations that for a simple switched-capacitor circuit as shown in Figure 21, the simulation result matches the derivation in section 2.1.4.2 and the integrated noise spectrum from 0 to *inf* will give approximately the same noise variance as was obtained from the computer simulation.

CHAPTER 3 NOISE CALCULATION FOR TWO WIDELY USED SC CIRCUITS

In Chapter 2, we reviewed the theorem that states that if the samples from each clock period are not correlated, than the variance of the continuous-time signal will be the same as the variance of the sampled discrete signal. In Chapter 2, both power spectral density (PSD) analysis and kT/C analysis for noise variance are discussed for low pass 1st order SC circuits. In mixed signal application, several SC circuits are widely used. The PSD of the noise of these circuits will be different for these circuit from that of the 1st order low pass filter. In the following chapters, a PSD analysis for the noise during the track phase and the continuous noise during the hold phase will be discussed for two widely used SC amplifier circuits, the flip-around amplifier and the charge-redistribution amplifier. First in this chapter, the PSD analysis will be derived for the noise during the track phase for both the flip-around structure and the charge-redistribution structure. Noise power calculated from PSD analysis will be compared to that from a conventional kT/C analysis.

3.1 Flip-around Structure

3.1.1 Derivation of the PSD of Noise by Method I

For the flip-around SC gain stage, we assume the non-dominant pole is far away from the dominant pole. With this assumption, we can look at the flip-around gain stage as a single-pole system. So the first-order derivation from the foregoing section still provides a good approximation to the spectral performance of the flip-around SC gain stage[22]-[25] and will be used in the following analysis.

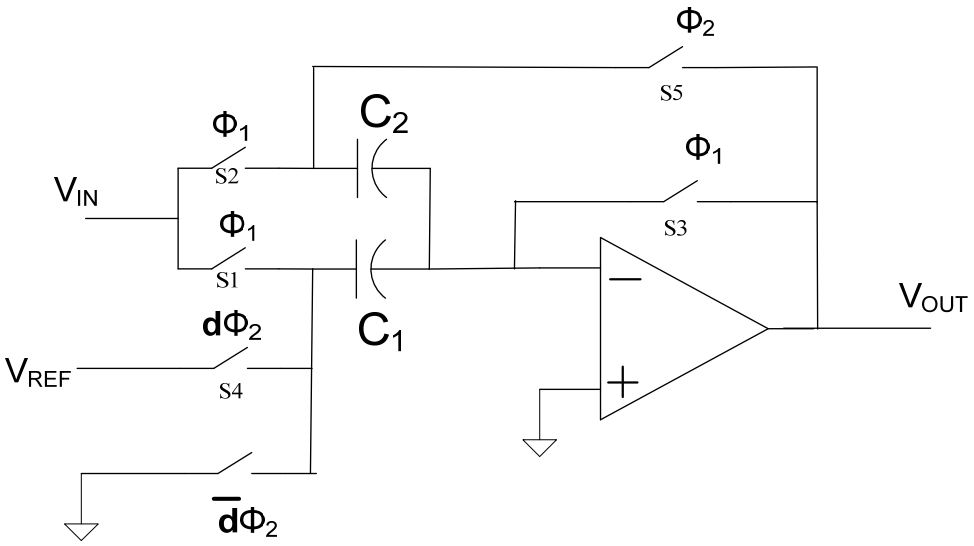


Figure 24. Flip-around switched-capacitor amplifier

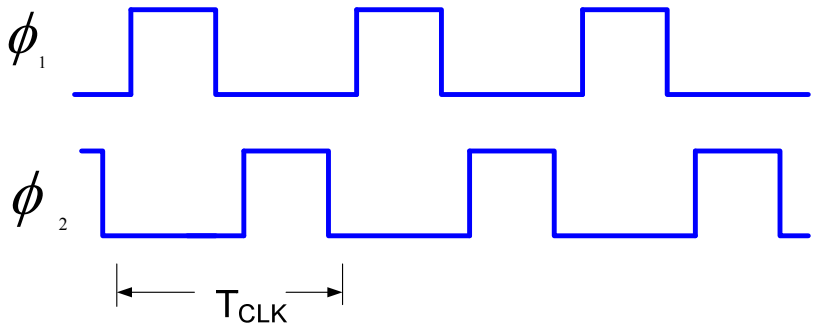


Figure 25. Clock signal

The non-overlapping clock signal is shown in Figure 25. When Φ_1 is high, the circuit is operating in the track mode and when Φ_2 is high, the circuit is operating in the hold mode phase.

During the phase Φ_1, the equivalent circuit is:

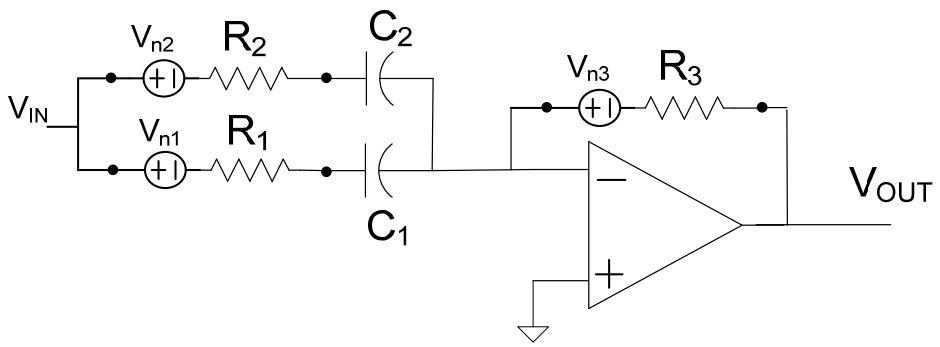


Figure 26. Circuits during the track phase

V_{n1} V_{n2} and V_{n3} are the noise source caused by the resistance of switch S_1, S_2 and S_3. R_1, R_2 and R_3 are the resistance of switches S_1, S_2 and S_3.

The transfer function of the operational amplifier is assumed to be:

$$H_{opamp}(s) = \frac{GB}{s} \tag{3.1}$$

The noise PSD of the output voltage during the phase Φ_1 will be determined by the noise generated by the resistances R_1, R_2, R_3 from switches S_1, S_2, and S_3. However, the output we are looking at is the output during the hold phase. So we don't care about the output noise during phase Φ_1, but we care about the noise at output during the hold phase Φ_2. During Φ_2, the switch S_3 is open so R_3 will not contribute to the output noise voltage. The noise that is present on the output during phase Φ_2 will be comprised of that sampled onto C_1 and C_2 during phase Φ_1 along with the continuous-time noise contributed by switches S_4 and S_5. Since the gain of the operational amplifier is large, S_3 will contribute little to the sampled noise on C_1 and C_2 during phase Φ_1.

This analysis will be restricted to the sampled noise on C_1 and C_2 that is the continuous-time noise contributed by S_4 and S_5 will be neglected.

The transfer function from V_{n1} or simply V_1 to the voltage across C_1 is:

$$H_1(s) = \frac{V_{c1}}{V_1} = \frac{s^2(R_3C_2 + R_2C_2) + s(R_2C_2GB + 1) + GB}{sC_1(1+sR_2C_2)sR_3 + sC_2(1+sR_1C_1)sR_3 + (s+GB)(1+sR_1C_1)(1+sR_2C_2)} \tag{3.2}$$

The square of magnitude of the transfer function is:

$$\left|H_1(j\omega)\right|^2 = \frac{\left(GB-\omega^2\left(R_3C_2+R_2C_2\right)\right)^2+\left(\omega^2\left(R_2C_2GB+1\right)^2\right)}{\left[GB-\omega^2\left(C_1R_3+R_3C_2+R_1C_1R_2C_2GB+R_2C_2+R_1C_1\right)\right]^2+\left[\omega\left(1+R_1C_1GB+R_2C_2GB\right)-\omega^3\left(2C_1R_2C_2R_3+R_1C_1R_2C_2\right)\right]^2} \tag{3.3}$$

From (3.3), we can numerically calculate $\left|H_1(j\omega)\right|^2 = \frac{1}{2}$, to obtain 3dB frequency, $\omega_{3dB,}$ and substitute this into equation (2.20), we can get noise PSD at C_1.

From V_{C1} to Vout, we have

$$H(z) = \frac{C_1}{C_2}z^{-1} \tag{3.4}$$

$$H_{c1\to o}(j\omega T_c) = \frac{C_1}{C_2}e^{-j\omega T_c} \tag{3.5}$$

Since the noise PSD in phase Φ_1 at C_1 is

$$S_{h\_c1}(f) = (1-\alpha)^2\frac{\omega_{3dB1}}{f_c}kTR_1\,\mathrm{sinc}^2\left(\frac{(1-\alpha)2\pi f}{2f_c}\right) \tag{3.6}$$

The hold phase noise PSD at the output will be:

$$S_{no1}(f) = S_{n\_c1}\left|H_{c1\to o}(j\omega)\right|^2 \tag{3.7}$$

Thus, $S_{no1}(f)$ can be expressed as

$$S_{no1}(f) = (1-\alpha)^2\frac{\omega_{3dB1}}{f_c}kTR_1\,\mathrm{sinc}^2\left(\frac{(1-\alpha)2\pi f}{2f_c}\right)\left(\frac{C_1}{C_2}\right)^2 \tag{3.8}$$

By a similar method we can get noise at output from switch 2.

$$H_{c2\to o}(j\omega T_c) = e^{-j\omega T_c} \tag{3.9}$$

Thus, $S_{no2}(f)$ can be expressed as

$$S_{no2}(f) = (1-\alpha)^2\frac{\omega_{3dB2}}{f_c}kTR_2\,\mathrm{sinc}^2\left(\frac{(1-\alpha)2\pi f}{2f_c}\right) \tag{3.10}$$

At very low frequencies:

$$S_{no}(0) = S_{no1}(0)+S_{no2}(0) = (1-\alpha)^2\frac{kT}{f_c}\left(\omega_{3dB2}R_2+\omega_{3dB1}R_1\left(\frac{C_1}{C_2}\right)^2\right) \tag{3.11}$$

The sampled RMS noise voltage at output during phase Φ_2 is equal to:

$$V_{o\_rms} = \sqrt{\int_0^{\infty} \left(S_{no1} + S_{no2}\right) df} \,/\left(1-\alpha\right) \tag{3.12}$$

If we sample the output of the SC gain stage, then the noise PSD of the output sequence becomes:

$$S_{SAM} = \frac{kT}{f_c}\left(\omega_{3dB1} R_2 + \omega_{3dB2} R_1 \left(\frac{C_1}{C_2}\right)^2\right) \tag{3.13}$$

3.1.2 Simulation Result

The schematic used for simulation is shown in Figure 27. The switches and the Op Amp are realized with VerilogA code. Resistors in series with the switches are used to model the turn-on resistance of the switches.

Parameters used in the circuit are shown in Table 2:

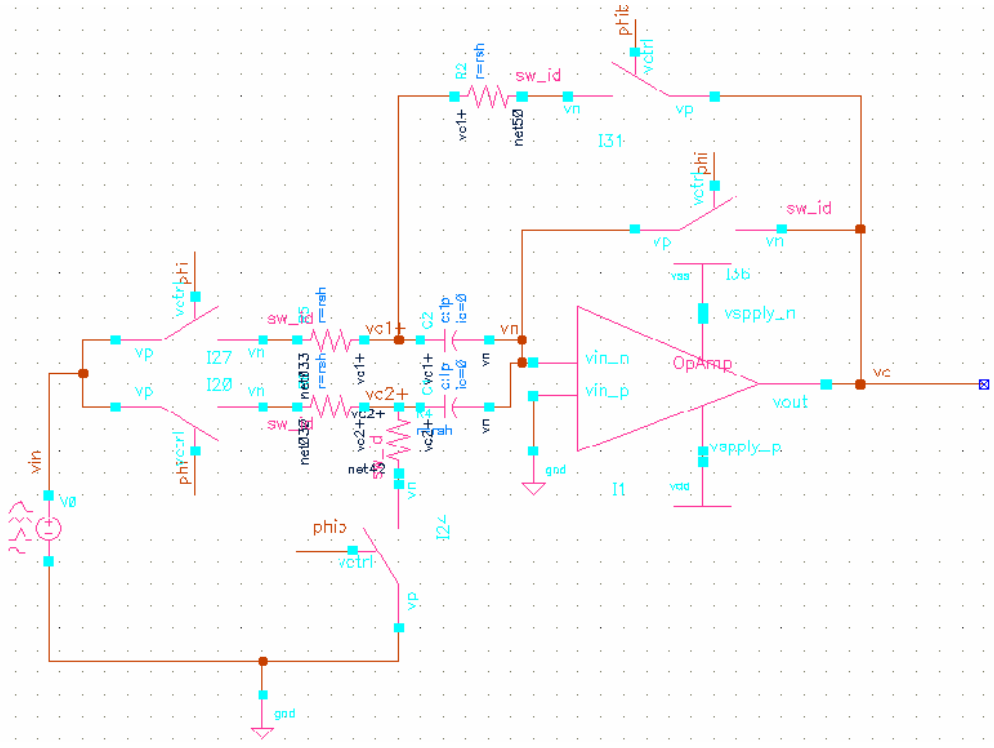


Figure 27. Flip-around simulation schematic

Table 2. Simulation parameters

Components	value
$R_1, R_2,$	10kΩ
R_3, R_4, R_5	0
C_1, C_2	1pF
GB (of Op Amp)	1MHz
f_c	10KHz
α	0.5

Hence it follows that

$\beta = C_2/(C_1+C_2) = 0.5$

$\theta = R_2 C_2 \beta GB = 1$

Simulation results for the noise PSD at the output are shown in Figure 28. From the simulation results, it can be observed that S(0)≈125nV/sqrt(Hz).

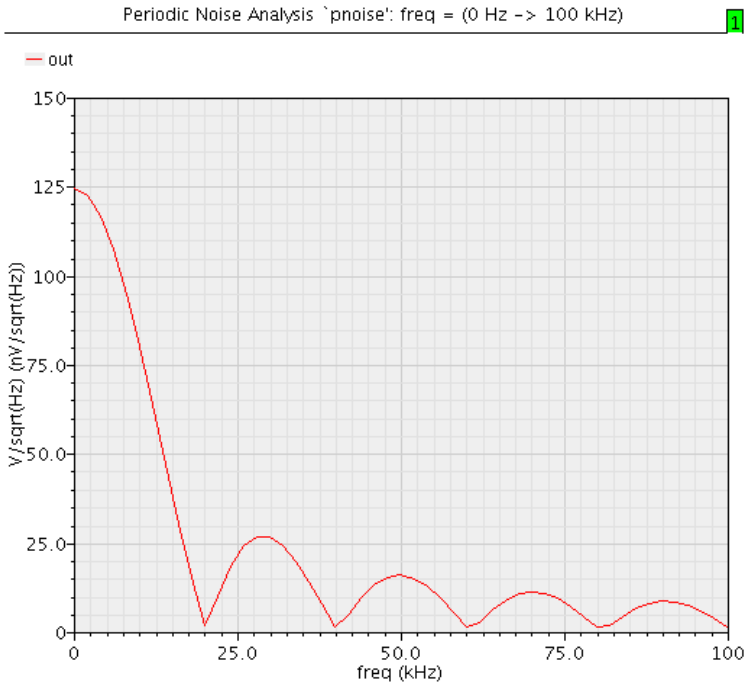


Figure 28. Noise spectrum during hold phase

From (3.2) and the corresponding expression for $H_2(s)$, w_{3dB1} and w_{3dB2} were numerically determined and were identical and given by $\omega_{3dB}=7.7596\times10^6$rad/sec

From equation (3.11), the noise during hold phase at low frequency is equal to

$$\sqrt{S_o(0)} = \sqrt{0.5^2 \frac{7.7596\times10^6}{10^4} kT\left(10^4+10^4\right)} = 126.77nV/\sqrt{Hz} \tag{3.14}$$

This closely matches the simulation result in Figure 28. According to equation (3.13), the sample noise at the output has noise PSD given by:

$$\sqrt{S_s} = 358.55nV/\sqrt{Hz} \tag{3.15}$$

The corresponding simulation results are shown in Figure 29. This analytical result is a little larger than the simulated result shown in Figure 29 which is about 320nV/ $/\sqrt{Hz}$. This difference is due, in part, to the first-order model used to characterize the performance of a 3rd-order system. Although there is a modest difference between the simulation results and the calculation, the simulation results are still in reasonable agreement with the hand calculation.

From equation (3.12), we can get the noise variance at the output, $\overline{v}_{o\_rms} = 45.255\mu V$. Refer it back to the input of the circuit, the input referred noise variance will be $\overline{v}_{in\_rms} = 22.63\mu V$.

From another point of view, during phase Φ_1, the noise from switches is sampled onto the capacitors. During the hold phase Φ_2, the noise sampled on the capacitors is viewed as DC voltage source and be amplified by the Op Amp to the output.

By kT/C analysis, we can get noise variance at output at the end of the hold phase Φ_2 and then referred it back to the input.

$$\overline{v}_{o\_rms} = \sqrt{\frac{\beta kT}{C_1} + \frac{kT}{C_2}} \tag{3.16}$$

Referred the noise at output back to the input, $v_{in\_rms} = 37.38\mu V$. The input referred noise calculated from kT/C analysis is different from PSD analysis since the circuit is not a

true one pole system. And the rectangular approximation is not accurate any more. But the result from kT/C analysis has the same order of magnitude to that from PSD analysis.

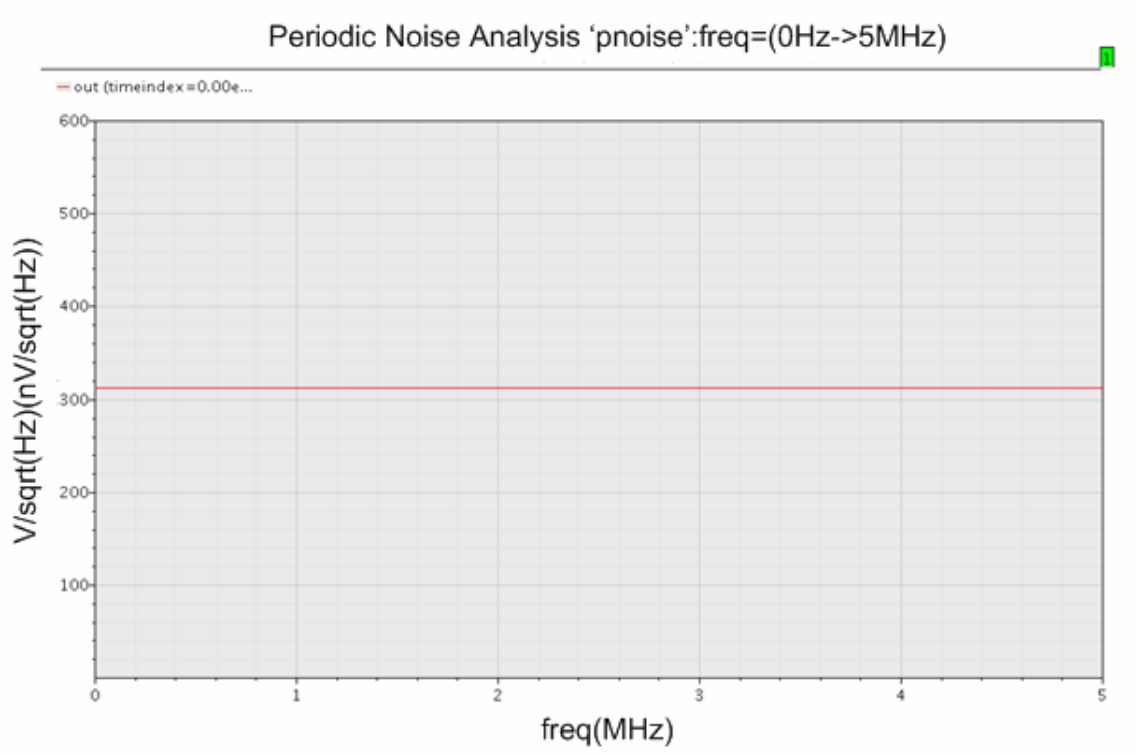


Figure 29. Sampled noise spectrum at the end of hold phase

3.1.3 Comparison

For the simplest SC circuit (Figure 15), although the expression for the PSD analysis are the same as the that of the kT/C analysis (see equation (2.24)), The expression of PSD analysis and kT/C analysis are substantially different for the flip-around SC gain stage. It is not clear how these two expressions compare. Hence, numerical comparison will be used for flip-around circuit.

It is shown numerically that the RMS values of the input referred noise calculated from a PSD analysis and the kT/C equations are of the same order of magnitude for both the flip-around switched-capacitor gain stage.

3.1.4 Derivation of the PSD of Noise by Method II

Second method is to calculate the real effective noise bandwidth f_{eff} and substituting it into equation (2.19).

In the second method, we have to first calculate the effective noise bandwidth f_{eff} so that the total power of the effective one is the same as the original one. That is:

$$S_{n1}(f) = 2kTR_1 \left| H_1(j2\pi f) \right|^2 \tag{3.17}$$

$$\int_{-\infty}^{\infty} S_{n1}(f)\,df = \int_{-\infty}^{\infty} 2kTR_1 \left| H_1(j2\pi f) \right|^2 df = 2kTR_1 f_{eff1} \tag{3.18}$$

From equation (3.18) we can get f_{eff1}. Then substituting into equation(2.19), we can get sampled noise PSD at C_1 $S_{n\_c1}(f)$. By the same way, we can get $S_{n\_c2}(f)$ and get V_{o_rms} by (3.7) and(3.12).

If the two poles of the gain stage are really close to each other. Then this method will be more accurate.

3.2 Charge-redistribution Structure

Another popular amplifier used in pipelined ADC stages is shown in the following Figure 30. As the flip-around structure and it also uses non-overlapping clocks. An advanced phase, Φ_{1A} is also added to provide for the bottom-plate sampling.

3.2.1 Derivation of the PSD of Noise

A PSD analysis for this charge-redistribution SC gain stage is similar to that used for the flip-around SC gain stage. So we will just list the key equations for this charge-redistribution structure.

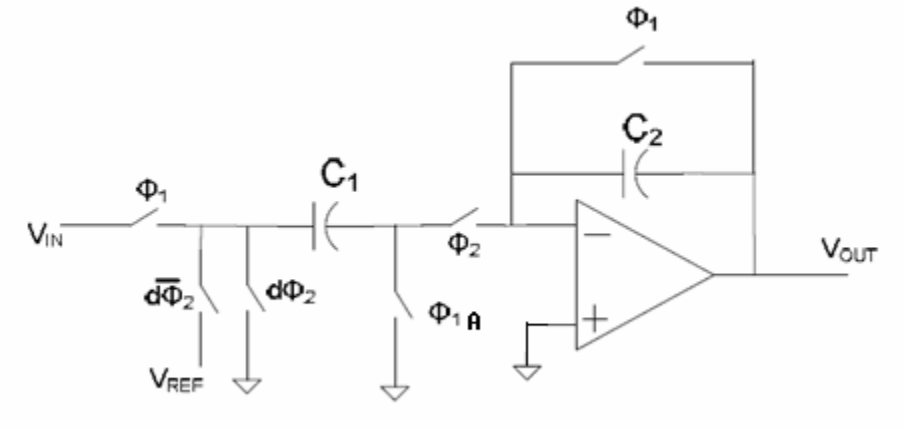


Figure 30. Basic switched-capacitor flip-around gain stage

During track phase Φ_1, the equivalent noise circuit is as shown in Figure 32:

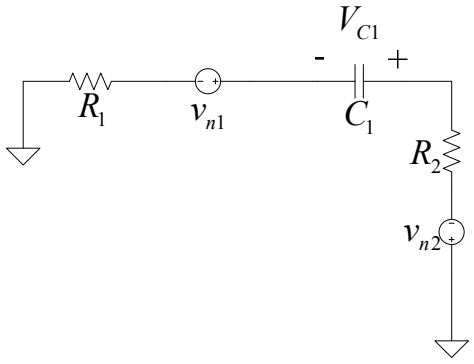


Figure 31. Equivalent circuit in track phase

$$V_{c1} = (V_{n1} + V_{n2}) \frac{\frac{1}{SC_1}}{R_1 + R_2 + \frac{1}{SC_1}}$$

$$= (V_{n1} + V_{n2}) \frac{1}{(R_1 + R_2) SC_1 + 1} \tag{3.19}$$

Hence the 3dB noise frequency of this first-order circuit is $1/((R_1+R_2)C_1)$.

During hold phase Φ_2, the equivalent circuit is as shown in Figure 32:

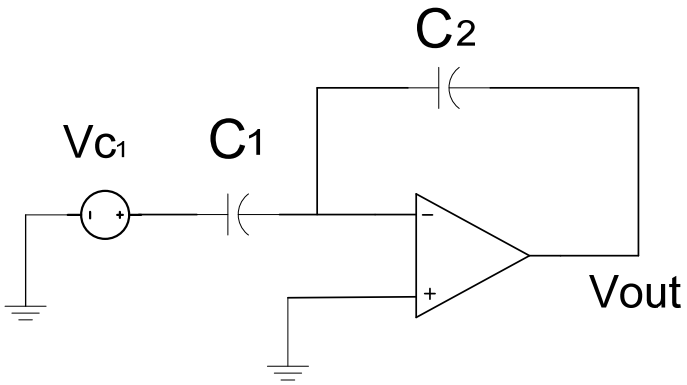


Figure 32. Equivalent circuit in hold phase Φ_2

The transfer function from V_{C1} to the output, is:

$$H\left(j\omega T_c\right)=\frac{-C_1}{C_2}e^{-j\omega T_c} \tag{3.20}$$

Hence the single-sided output noise PSD during the hold phase Φ_2 is:

$$\begin{aligned} S_{nh}\left(f\right)&=\left(1-\alpha\right)^2\frac{\omega_{3dB}}{f_c}kT\left(R_1+R_2\right)\mathrm{sinc}^2\left(\frac{\left(1-\alpha\right)\cdot 2\pi f}{2f_c}\right)\left|H\left(j\omega\right)\right|^2 \\ &=\left(1-\alpha\right)^2\frac{kT}{C_1}\sin c^2\left(\frac{\left(1-\alpha\right)\cdot 2\pi f}{2f_c}\right)\left|H\left(j\omega\right)\right|^2 \end{aligned} \tag{3.21}$$

At very low frequency, the PSD becomes:

$$S_{nh}\left(0\right)=\left(1-\alpha\right)^2\frac{kT}{C_1f_c}\left(\frac{C_1}{C_2}\right)^2 \tag{3.22}$$

If we sample the output at the end of hold period, we can get:

$$S_{SAM}\left(f\right)=\frac{kT}{C_1f_c}\left(\frac{C_1}{C_2}\right)^2 \tag{3.23}$$

As for charge-redistribution SC gain stage, during track phase Φ_1, the Op Amp is disconnected from the input. So the components connected to the input form just a RC circuit and the spectrum is the same as the 1st order low pass filter. So the analysis and simulation results for 1st order low pass filter shown in Chapter 2 are also valid for charge distribution structure.

Hence, during the track phase Φ_1, the noise from switches is sampled onto the capacitors. During the hold phase Φ_2, the noise sampled on the capacitors can be viewed as DC voltage source and be amplified by the Op Amp to the output.

By using kT/C analysis, we can get noise variance at output at the end of the hold phase and then referred it back to the input.

3.3 Comparison between PSD Analysis and kT/C Analysis

Numerical comparison between results from kT/C analysis and PSD analysis for both circuits is shown in Figure **33** and Figure **34**. The result shows the RMS value from PSD analysis depends only on the product θ=RCβGB and feedback factor β.

If $\theta \gg 1$, then 1/RC is the dominant pole. Vice versa, $\theta \ll 1$, GB of Op Amp is the dominant pole of the system. θ will be discussed in detail in the following chapter.

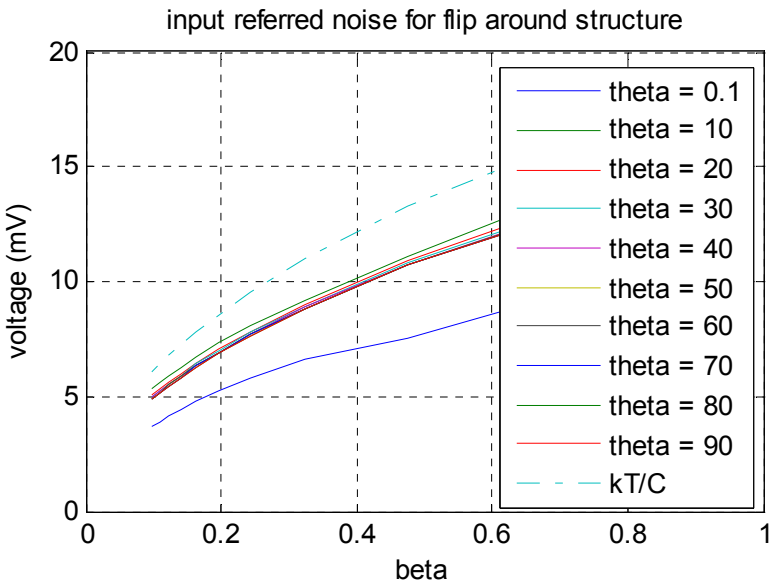


Figure 33. S/H noise of flip-around structure

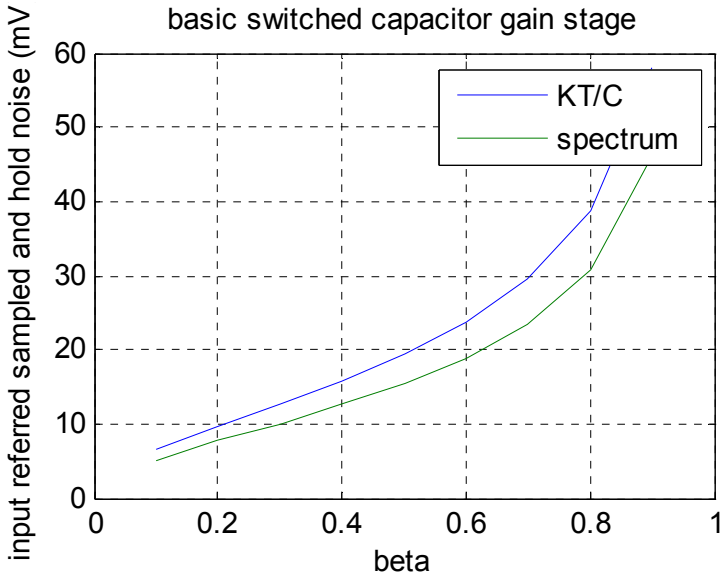


Figure 34. S/H noise of basic structure

In Figure **33**, when θ>1, the result from kT/C analysis is 20% larger than PSD analysis because the approximation for 3dB bandwidth is used in PSD analysis. But it is still reasonably close to PSD analysis. Hence, the analysis for S/H noise in a switched-capacitor circuit will not deviate a lot from the real value by using kT/C analysis without considering sampling effect and aliasing. However, in Figure **33**, when θ=0.1, curve from the kT/C analysis does not match curve from the PSD analysis. That is because when θ is so small, the bandwidth of the system is determined by the gain bandwidth product of the Op Amp, so the bandwidth of thermal noise is much less than 1/RC and the total noise variance is reduce by the bandwidth limitation. In the Figure **34**, as the GB of Op Amp will not affect the bandwidth of the S/H noise in the sampling phase, so the noise variance is independent of the figure of merit θ.

Although the PSD analysis shows the total S/H noise variance will be smaller than variance gotten from kT/C analysis in some cases, we will still use kT/C analysis in next chapter for simplicity. But we will keep it in mind that the variance will be smaller than that calculated from kT/C analysis if the GB of Op Amp dominated the bandwidth of the circuit.

3.4 Conclusion

In this chapter, we have derived the PSD for both flip-around SC circuits and Charge-redistribution circuits. Cadence SpectreRF is used to evaluate the PSD hand analysis. It has been shown that the simulation results match the analysis reasonable well. Matlab simulation results show that if the thermal noise is undersampled, it can used DC voltage to represent S/H circuits with reasonable accuracy. So in the next chapter, for simplicity, we will directly use the DC voltage source to replace the S/H noise source and start to talk about the continuous noise of the circuits.

CHAPTER 4 CONTINUOUS-TIME NOISE ANALYSIS

For switched-capacitor circuits, thermal noise from the track phase or the S/H noise is widely characterized by a standard "kT/C" noise analysis. Noise from the hold phase has not been discussed; however, the noise contribution from hold phase can be very important, and depends on the GB of the amplifier, feedback factor and so on. As the noise generated during the hold phase will not be sampled on the sample clock and appears as a continuous-time signal, it will be called continuous-time noise in this thesis. If a switched-capacitor stage is followed by another SC circuit, the continuous-time noise itself will be sampled; is sampled noise will be further discussed. In this chapter, the continuous-time (CT) noise present during hold phase will be discussed and compared to the S/H noise. The contribution of the CT noise will be discussed for both the flip-around and charge-redistribution SC circuits.

4.1 Introduction

In the previous chapter, the power spectral density of noise generated during the track phase was analyzed for both the flip-around structure and the charge-redistribution structure. Integrating the PSD from w=0 to infinity, we showed that the total noise power is of the same of magnitude as that calculated from standard kT/C analysis. So in this chapter, for simplicity we will use kT/C analysis to analyze the noise from track phase. Then the continuous-time noise will be calculated and compared to the noise present from the sampling phase. The two most widely used SC amplifier circuits will be used in this chapter.

4.2 Figure of Merit θ

Some discussion about the characteristics of the noise voltage at the output of the S/H circuit is in order. For proper operation of this circuit, it is necessary that the settling time of

the $R_{SW}C$ circuits be small compared to the clock period T_{CLK} and it is necessary that the GB of the op amp must be much larger than f_{CLK}. These requirements can be expressed as

$$T_{CLK} >> R_{SW}C \tag{4.1}$$

$$T_{CLK} >> 1/GB \tag{4.2}$$

These requirements do not place restrictions on the relationship between the GB of the op amp and the settling time of the passive part of the circuit, $R_{SW}C$. In the following paragraphs, we will quantitively discuss the relationship between amplifier BW and the size of the switches.

4.2.1 Amplifier Gain and BW Requirements

The operational amplifier must be fast enough to provide adequate settling in the clock period of the amplifier and, if calibration is not needed, must have enough dc gain to guarantee the settled value of the feedback amplifier output is close enough to the desired value. The linearity of the amplifier also affects performance and the gain should be kept sufficiently high throughout the output signal swing range.

The op amp can generally be modeled with the first-order gain expression

$$A(s) = \frac{A_0 p}{s + p} \cong \frac{GB}{s} \tag{4.3}$$

The dc gain is given by A_0 and the high frequency response and, in particular the settling time of the feedback amplifier, is characterized by the gain-bandwidth product GB. Beyond meeting phase margin requirements, there is little concern about the pole location p.

When feedback is applied, the β of the feedback network is often modestly different than the reciprocal of the dc gain and this must be taken into account when doing compensation and when analyzing the performance of the finite gain stages.

The gain of a feedback network can be expressed as

$$A_{FB} = \frac{A\eta}{1 + A\beta} \tag{4.4}$$

where the desired feedback gain is η/β. The minimum dc gain is often specified so that the settled error is less than ½ LSB relative to the effective number of bits of resolution that must be retained at the output of the amplifier stage. Mathematically this requirement can be expressed as.

$$\frac{A\eta}{1+A\beta} = (1-\frac{1}{2^{n_{ST}+1}})\frac{\eta}{\beta} \tag{4.5}$$

where n_{ST} is the effective resolution expressed as the number of equivalent binary bits.

This can be solved for the minimum acceptable gain A which can be expressed as

$$A_{dB} \cong 6n_{ST} + 6 - 20\log(\beta) \tag{4.6}$$

The GB is generally selected to guarantee an acceptable settling time. The requirement that is usually established is that the worst-case settling must be to within ½ LSB in an interval of length T_X where T_X is the time available for the amplifier to settle. If slewing is neglected, worst-case settling will occur when the step is the largest. This is depicted in the following Figure **35** where it is assumed that the largest step at the output is V_{REF}.

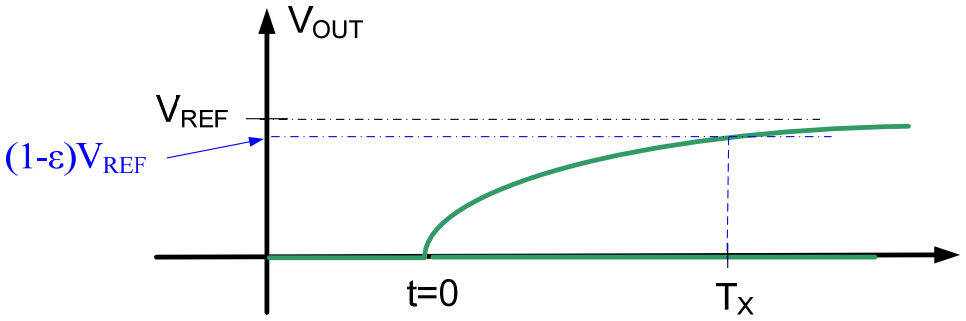


Figure 35. Settling of SC amplifier

In this figure ε characterizes the minimum acceptable settling error and is given by

$$\varepsilon = \frac{1}{2^{n_{ST}+1}} \tag{4.7}$$

Since the amplifier is a first-order feedback network, the response can be expressed in the form

$$r(t) = F + (I - F)e^{-\beta GBt_s} \tag{4.8}$$

where F is the final value and I is the initial value of the output waveform.

It thus follows that

$$V_{REF}(1-\varepsilon) = V_{REF}\left(1-e^{-\beta GBT_X}\right) \tag{4.9}$$

This can be solved for GB in terms of T_X to obtain

$$GB = -\frac{\ln(\varepsilon)}{\beta T_X} \tag{4.10}$$

Often the time interval for settling, T_X, is half of the clock period

$$T_X \cong \frac{T_{CLK}}{2} = \frac{1}{2f_{CLK}} \tag{4.11}$$

So, substituting for ε and T_X, we obtain

$$GB = \frac{(n_{ST}+1)2\ln 2}{\beta} f_{CLK} \cong \frac{1.4(n_{ST}+1)}{\beta} f_{CLK} \tag{4.12}$$

where the GB is in rad/sec.

4.2.2 Sizing of the Switches

The issue of how the switches should be sized does deserve attention. If the switch is sized to have a very small ON impedance, the area will be large (resistor value inversely proportional to the W/L ratio of the switch), the switch will be slow down, and the dynamic power needed to drive the switch will be high. If the switch ON impedance is too large, settling will not occur during the sampling interval. Once the switch sizing strategy is determined, the relationship between $R_{SW}C$ and GB can be determined and this will provide guidance on the switch noise during the "continuous-time" mode of operation of a sampling circuit.

Considering again the switch-capacitor sampler of Figure 15, there are two different conditions that may govern the settling requirements. One is in the track mode when the input signal is continuously varying and the other is in the sample mode where the input signal itself has already been sampled and is relatively constant during most of the sampling operation. These two cases will be considered separately.

If the input remains constant throughout the sampling operation the response can be represented by the step response of a first-order network as

$$r(t) = F + (I - F)e^{-\frac{t}{R_{SW}C}} \tag{4.13}$$

Assuming Nyquist-rate inputs, worst case settling will occur when the step is maximum which corresponds to I=0 and F=V_{REF}. If ε characterizes the worst-case acceptable setting, this must occur at time $T_{CLK}/2$. In this case, the settling waveform must satisfy the equation

$$V_{REF}(1 - \varepsilon) = V_{REF}\left(1 - e^{-\frac{T_{CLK}}{2R_{SW}C}}\right) \tag{4.14}$$

this can be solved for R_{SW} to obtain

$$R_{SW} = -\frac{1}{2Cf_{CLK}\ln(\varepsilon)} \tag{4.15}$$

If we assume the settling must be to ½ LSB at the n_{ST} level (this may not be quite good enough), then

$$\varepsilon = \frac{1}{2^{n_{ST}+1}} \tag{4.16}$$

Substituting this into the expression for R_{SW}, we obtain

$$R_{SW} = \frac{1}{Cf_{CLK}\,2\ln(2)(n_{ST}+1)} \tag{4.17}$$

which can be expressed as

$$R_{SW} = \frac{1}{Cf_{CLK}(1.386)(n_{ST}+1)} \tag{4.18}$$

This must be met for every switch-capacitor combination.

4.2.3 Second Order System

If an Op Amp with a first-order gain character is embedded in a 1st-order passive network, the resultant circuit becomes second-order. For the second order system shown in Figure **36**, if $R_1 = R_2 = R$, the transfer function can be written as

$$H(s) = \frac{\left(-\frac{R_2}{R_1}\right) p_1 p_2}{(s + p_1)(s + p_2)} \tag{4.19}$$

where $p_1 \approx GB$ and $p_2 \approx \frac{1}{RC}$.

The metric θ will be defined that relates the two poles in the amplifier by the expression.

$$\theta = RC\beta GB = \frac{p_1}{p_2} \tag{4.20}$$

If $\theta \gg 1$ and $p_1 \gg p_2$, then 1/RC is the dominant pole. Vice versa, if $\theta \ll 1$ and $p_1 \ll p_2$, the GB of the Op Amp is the dominant pole of the system.

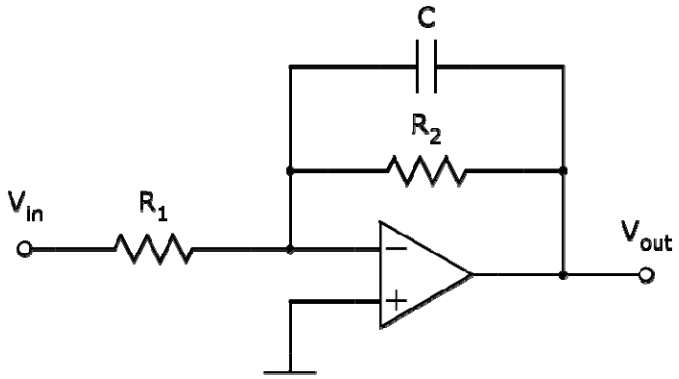


Figure 36. Lossy integrator

4.3 Flip-around Structure

Consider again the flip-around SC voltage amplifier repeated in Figure **37**. We will now consider the continuous-time noise at the output that is present during phase Φ_2.

During phase Φ_2 the circuit can be represented as shown in Figure **39** where $\overline{V}_{n1S}$ and $\overline{V}_{n2S}$ represent the samples of the switch noise that were taken at the end of phase Φ_1. The sampled input voltage and the sampled noise voltages obtained during phase Φ_1 are explicitly shown in this figure. It must be emphasized that some of the independent variables are dc voltage sources and others are time-varying noise sources that we are sampled at the end of phase Φ_1. The variable **d** is a Boolean variable that assumes an integer numerical value of 0 or 1. When **d**=0, V_{REF} would be replaced by a short to ground. If it is assumed that the gain of the amplifier is A(s)=GB/s, it follows from a routine but tedious analysis that the output in the frequency domain during phase Φ_2 domain can be expressed as

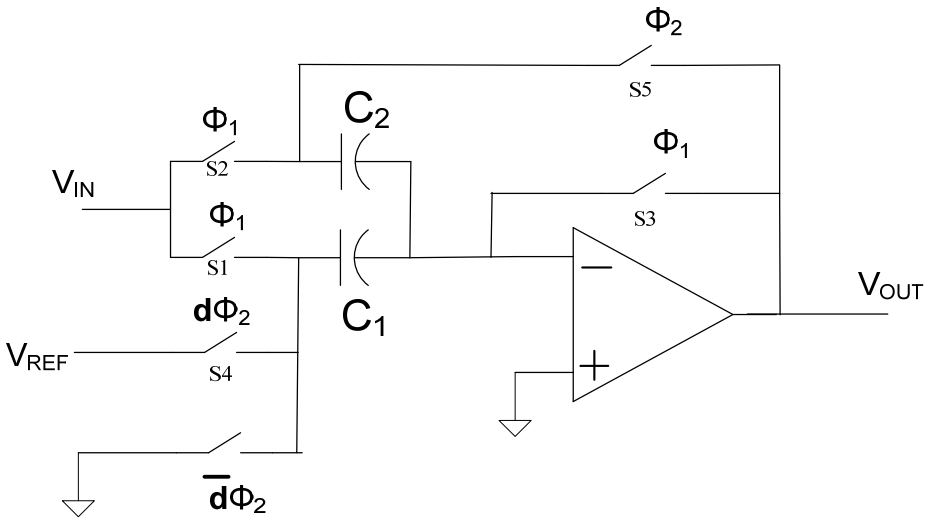


Figure 37. Flip-around SC circuit

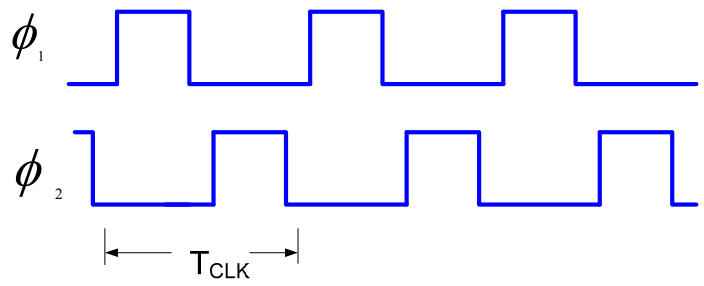


Figure 38. Clock signal

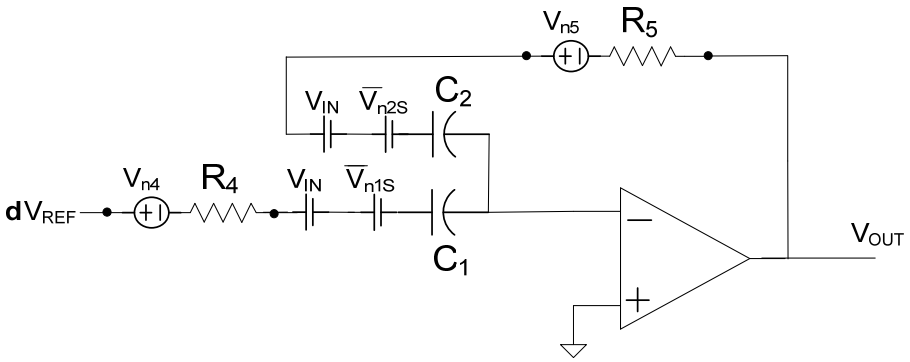


Figure 39. Switch noise sources in hold phase

$$V_{out} = V_{in}\left(\frac{1+\frac{C_2}{C_1}+sC_2(R_4+R_5)}{\frac{C_2}{C_1}+s\left[R_4C_2+\frac{1}{GB}\left(1+\frac{C_2}{C_1}\right)\right]+s^2\frac{1}{GB}(R_5+R_4)C_2}\right)$$
$$-d_1V_{REF}\left(\frac{1+R_5C_2s}{\frac{C_2}{C_1}+s\left[R_4C_2+\frac{1}{GB}\left(1+\frac{C_2}{C_1}\right)\right]+s^2\frac{1}{GB}(R_5+R_4)C_2}\right)$$
$$+\frac{\hat{V}_{n1}(1+R_5C_2s)+\hat{V}_{n2}\left(\frac{C_2}{C_1}(1+R_4C_1s)\right)}{\frac{C_2}{C_1}+s\left[R_4C_2+\frac{1}{GB}\left(1+\frac{C_2}{C_1}\right)\right]+s^2\frac{1}{GB}(R_5+R_4)C_2}$$
$$+\frac{\hat{V}_{n4}(1+R_5C_2s)-\hat{V}_{n5}\left(\frac{C_2}{C_1}(1+R_4C_1s)\right)}{\frac{C_2}{C_1}+s\left[R_4C_2+\frac{1}{GB}\left(1+\frac{C_2}{C_1}\right)\right]+s^2\frac{1}{GB}(R_5+R_4)C_2} \quad (4.21)$$

where the ^ on a variable indicates a sampled noise value. Assuming the clock frequency is slow enough that the amplifier settles, the output due to all of the dc components will settle to their steady-state value. The continuous-time noise sources, V_{n4} and $V_{n5,}$ are the only terms that will provide a time-varying output after the amplifier has settled. Under these settling assumptions, the expression for V_{OUT} simplifies to

$$V_{OUT}=V_{IN}\left(1+\frac{C_1}{C_2}\right)-\mathbf{d_1}V_{REF}\left(\frac{C_1}{C_2}\right)+\hat{V}_{n1}\left(\frac{C_1}{C_2}\right)+\hat{V}_{n2} + \frac{\hat{v}_{n4}\left(1+R_5C_2s\right)-\hat{v}_{n5}\left(C_2/C_1\left(1+R_4C_1s\right)\right)}{C_2/C_1+s\left[R_4C_2+\frac{1}{GB}\left(1+C_2/C_1\right)\right]+s^2\frac{1}{GB}\left(R_5+R_4\right)C_2} \tag{4.22}$$

This can be written functionally in the form

$$V_{OUT}=V_{IN}\left(1+\frac{C_1}{C_2}\right)-d_1V_{REF}\left(\frac{C_1}{C_2}\right)+\hat{V}_{n1}\left(\frac{C_1}{C_2}\right)+\hat{V}_{n2}+\hat{V}_{n4}f_4(s)-\hat{V}_{n5}f_5(s) \tag{4.23}$$

where the functions $f_4(s)$ and $f_5(s)$ are second-order polynomials in s given by

$$f_4(s)=\frac{1+R_5C_2s}{C_2/C_1+s\left[R_4C_2+\frac{1}{GB}\left(1+C_2/C_1\right)\right]+s^2\frac{1}{GB}\left(R_5+R_4\right)C_2}$$
$$f_5(s)=\frac{C_2/C_1\left(1+R_4C_1s\right)}{C_2/C_1+s\left[R_4C_2+\frac{1}{GB}\left(1+C_2/C_1\right)\right]+s^2\frac{1}{GB}\left(R_5+R_4\right)C_2} \tag{4.24}$$

Since the noise sources are uncorrelated, the output voltage is given by

$$\tilde{V}_{OUT\text{-}RMS}=\sqrt{kT\left(\frac{C_1+C_2}{C_2^2}\right)+V^2{}_{4\text{-}5RMS}} \tag{4.25}$$

$$V_{4\text{-}5RMS}=\sqrt{4kT}\sqrt{\int_{f=0}^{\infty}\left(R_4\left|f_4(s)\right|^2+R_5\left|f_5(s)\right|^2\right)df}$$
$$=\sqrt{4kTR_4\left(1+\gamma\left(\frac{\beta}{1-\beta}\right)^2\right)}\sqrt{\int_{f=0}^{\infty}\left|f_4(s)\right|^2df} \tag{4.26}$$

where β is the feedback factor, $\beta=C_2/(C_1+C_2)$ and where γ is the ratio between R_5 and R_4, that is, $\gamma=R_5/R_4$.

The notation of the output RMS output voltage needs some interpretation since it is showing both continuous-time quantities expressed in RMS and values that are not time varying during phase Φ_2. Specifically, the first term on the RHS of the expression (4.25) is due to the sampled voltage obtained during phase Φ_1 and is not time varying. The second term, $V_{4\text{-}5RMS}$, is a time-varying term expressed in RMS. If the output is sampled, the sampled value will have the RMS value obtained from this equation by taking the sum of the squares of the two terms. To emphasize the mixed notation in this equation, the ~ was included on the symbol.

Thus from (4.25) the input referred noise voltage during phase Φ_2 is

$$\tilde{V}_{IN\text{-}RMS\phi_2} = \frac{C_2}{C_1}\left(\sqrt{kT\left(\frac{C_1+C_2}{C_2^2}\right)+V^2_{4\text{-}5RMS}}\right) \tag{4.27}$$

But, the input-referred noise voltage during phase Φ_2 is of little interest. What we are really interested in is the input referred noise voltage during phase Φ_1. Since the gain from the input to the output is $(C_1+C_2)/C_2$, we must divide the RMS output noise voltage by this gain to find the input-referred noise voltage.

When the output is sampled, the equivalent input referred noise voltage is the sample with RMS value.

$$\hat{V}_{IN\text{-}RMS} = \frac{C_2}{(C_1+C_2)}\sqrt{kT\left(\frac{C_1+C_2}{C_2^2}\right)+\hat{V}^2_{4\text{-}5RMS}} \tag{4.28}$$

It can be observed from the second-order term in the denominator of (4.24) that the magnitude of the gain will drop off at high frequencies thus limiting the noise power at the output. However, if the capacitors are in the pF range and the switch impedances are in the KΩ range, then the $R_{SW}C$ products are in the nsec range and could be comparable to or larger than the GB terms in $f_4(s)$ and $f_5(s)$ and the RMS noise voltage at the output of the op amp

can be quite large. Many authors simply ignore the noise contributed by R_4 and R_5 and this is justifiable provided the switch impedances are sufficiently small and, in this case, (4.28) reduces to $\hat{V}_{IN\text{-}RMS} = \sqrt{\frac{kT}{C_1 + C_2}}$.

If we assume $R_4C_1=R_5C_2$ and substitute equation (4.20) into equation (4.26), equation (4.26) can be written as

$$V_{4\text{-}5RMS} = \sqrt{\frac{4kT}{C_1\beta GB}\left(\frac{\theta}{1-\beta}\right)}\sqrt{\int_{f=0}^{\infty}\left(\left|f_4(s)\right|^2\right)df} \tag{4.29}$$

where the figure of merit $\theta = R_4C_1\beta GB$ defines the relationship between RC and βGB (explained in section 4.2.3) .

Substituting for the RC products of (4.20) into (4.24), we obtain the equivalent expressions:

$$f_4(s) = \frac{1-\beta}{\beta}\frac{1+s\frac{1}{\beta GB}}{1+s\left[\frac{1+\theta}{\beta GB}\right]+s^2\frac{\theta}{\beta GB^2}} \tag{4.30}$$

$$f_5(s) = \frac{\beta}{1-\beta}f_4(s)$$

Substituting the value for $f_4(s)$ into (4.29), replacing s with $j2\pi f$, and doing a variable substitution, it follows that

$$V_{4\text{-}5RMS} = \sqrt{\frac{2kT\theta(1-\beta)}{C_1\beta^2\pi}}\sqrt{\int_{f=0}^{\infty}\frac{1+\theta^2f^2}{\theta^2\beta^2f^4+\left[(1+\theta)^2-2\theta\beta\right]f^2+1}df} \tag{4.31}$$

Although not apparent from the expressions, it has been observed by simulations that with β=½, the definite integrals will be identical with different θ but they differ when β differs from ½. With this observation, for β=½, we can obtain

$$V_{4\text{-}5RMS} = \sqrt{\frac{4kT\theta}{C_1\pi}}\sqrt{\int_{f=0}^{\infty}\frac{1}{1+f^2}df} = \sqrt{\frac{\theta 2kT}{C}} \tag{4.32}$$

$$\hat{V}_{IN\text{-}RMS} = \sqrt{\left(\frac{kT}{2C}\right)+\left(\frac{\theta kT}{2C}\right)} = \sqrt{\frac{kT}{C\left[\frac{2}{1+\theta}\right]}} \tag{4.33}$$

where β=½, $C=C_1=C_2$. If θ=1, then equation (4.33) becomes

$$V_{4\text{-}5RMS} = \sqrt{\frac{4kT}{C\pi}}\sqrt{\int_{f=0}^{\infty}\frac{1}{1+f^2}df} = \sqrt{\frac{2kT}{C}} \tag{4.34}$$

When referred back to the input, this becomes

$$\hat{V}_{IN\text{-}RMS} = \sqrt{\left(\frac{kT}{2C}\right)+\left(\frac{kT}{2C}\right)} = \sqrt{\frac{kT}{C}} \tag{4.35}$$

The first term under the radical is due to the noise during phase Φ_1 and the second term is due to the noise during phase Φ_2. In this case, the second phase contributes just as much noise as the first phase which is not an attractive property since it significantly increases the size of the input capacitors needed to meet a given noise requirement.

Table 3. Noise contributions of switches during Φ_2

		β		
		1/2	1/4	1/8
θ=1	$V_{4\text{-}5RMS}$	1.414	2.24	3.31
	$V_{IN\text{-}RMS}$	1	1.03	1.02
	C_{INEQ}	C_1	$0.94C_1$	0.95C1
θ=1/2	$V_{4\text{-}5RMS}$	1	1.79	2.83
	$V_{IN\text{-}RMS}$	0.87	0.97	1
	C_{INEQ}	$(4/3)C_1$	$1.05C_1$	C1
θ=1/4	$V_{4\text{-}5RMS}$	0.707	1.414	2.41
	$V_{IN\text{-}RMS}$	0.79	0.94	0.98
	C_{INEQ}	$(8/5)C_1$	$1.14C_1$	1.04C1
θ=0	$V_{4\text{-}5RMS}$	0	0	0
	$V_{IN\text{-}RMS}$	0.707	0.87	0.94
	C_{INEQ}	$2C_1$	$1.33C_1$	1.14C1

Table 3 summarizes the contributions to the sampled input refined noise as a function of both β and θ. They are expressed as the factor that must multiply the term $\sqrt{kT/C}$. Also shown in the table is the effective sampling capacitance.

From Table 3, it can be observed that the sizing of the switches does play a key role in the overall noise and that just making the switches small enough to meet settling performance requirements does still result in a rather substantial excess noise introduced by the Φ_2 switches. Making the switches large and correspondingly, the switch impedance small to reduce their contribution, however, may not be particularly attractive either.

From this table, it should be apparent that the switches can add significant noise during the charge transfer stage (i.e. second phase) that will be sampled by the following stage. This noise increases the size needed for the sampling capacitor. Of course, if θ is small enough this noise will become negligible.

Keeping everything the same but reducing the size of the switches will increase θ as the resistance of the switches is increased. However, as stated said in previous chapters, for some applications, the physical size of the switches has to be kept small to provide high speed or low dynamic power dissipation. For some applications, even minimum-sized transistors will provide a small enough value of θ to effectively eliminate the extra noise introduced during phase Φ_2 whereas other applications may require very large switches even if θ=1.

We will now determine the critical switch impedance as a function of the clock speed and the resolution of a data converter. It will be assumed that the time allocated to settling time is half of the clock period, that slewing can be neglected, that the RMS noise voltage can be at most ½ LSB with a V_{REF} of 1V, and that all of the sampling noise is determined by the capacitor C_1. With these assumptions, from the expressions for R_4, GB and the kT/C noise, repeated below, we obtain the expression for R_4.

For θ =1, we can calculate

$$R_4 = \frac{1}{C_1 \beta GB},$$
$$\sqrt{\frac{kT}{C_1}} = \frac{1V}{2^{n+1}} \tag{4.36}$$
$$GB = \frac{(n_{ST}+1)2\ln 2}{\beta} f_{CLK}$$

substituting into R_4, we will obtain

$$R_4 = \frac{1}{kT 2^{2n_{ST}+2}(n_{ST}+1)2\ln 2 f_{CLK}} \tag{4.37}$$

Table 4. Critical Switch Resistances for Continuous-Time Noise Accumulation

	Frequency						
Resolution	100	1K	10K	100K	1M	10M	100M
8	2.95E+11	2.95E+10	2.95E+09	2.95E+08	2.95E+07	2.95E+06	2.95E+05
9	6.64E+10	6.64E+09	6.64E+08	6.64E+07	6.64E+06	6.64E+05	66435
10	1.51E+10	1.51E+09	1.51E+08	1.51E+07	1.51E+06	1.51E+05	15099
11	3.46E+09	3.46E+08	3.46E+07	3.46E+06	3.46E+05	34602	3460.2
12	7.99E+08	7.99E+07	7.99E+06	7.99E+05	79850	7985	798.5
13	1.85E+08	1.85E+07	1.85E+06	1.85E+05	18537	1853.7	185.37
14	4.33E+07	4.33E+06	4.33E+05	43252	4325.2	432.52	43.252
15	1.01E+07	1.01E+06	1.01E+05	10137	1013.7	101.37	10.137
16	2.39E+06	2.39E+05	23852	2385.2	238.52	23.852	2.3852
17	5.63E+05	56318	5631.8	563.18	56.318	5.6318	0.56318
18	1.33E+05	13338	1333.8	133.38	13.338	1.3338	0.13338
19	31679	3167.9	316.79	31.679	3.1679	0.31679	0.031679
20	7542.6	754.26	75.426	7.5426	0.75426	0.075426	0.007543

From Excel, we obtain the critical values of R_4 indicated in the Table 4 at which the noise contribution from phase Φ_2 will be the same as the noise contribution from phase Φ_1. From Table 4, it should be apparent that throughout much of the range, the switches will have impedances much smaller than the critical impedance and consequently the continuous-time noise associated with the switches during the transfer mode will play little role and the

overall noise will be dominated by the switching noise. It can be observed, however, that at higher speeds and higher resolutions (shown in the green region), the continuous-time noise will be of concern as well.

4.4 Charge-redistribution Structure

For the charge-redistribution SC gain stage, shown again in Figure 40, we can derive a set of equations which are similar to those we obtained for the flip-around structure. The clock phasing is as given in Figure **38**.

This structure has a nominal gain of

$$A_{FB} = -\frac{C_1}{C_2} \tag{4.38}$$

And a feedback factor for the amplifier of

$$\beta = \frac{C_2}{C_1 + C_2} \tag{4.39}$$

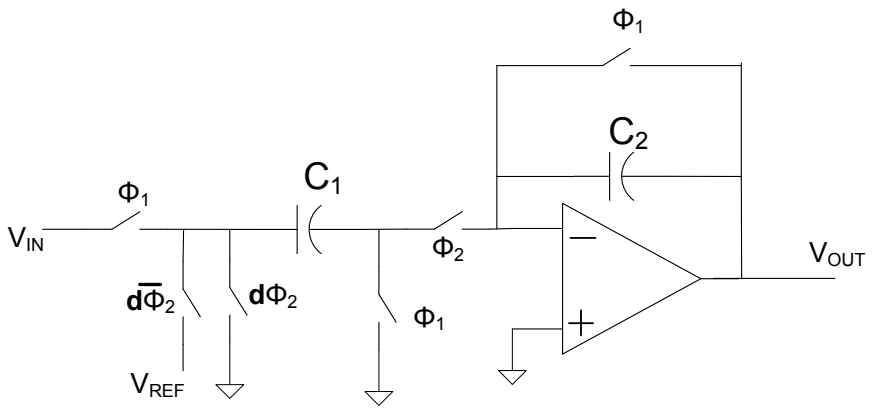


Figure 40. Basic Switched-Capacitor Gain Stage

The noise sources present during hold phase Φ_2 are shown in the following figure.

The sampled noise source present during phase Φ_1, denoted at V_{n1S}, has an RMS value of $\sqrt{kT/C_1}$.

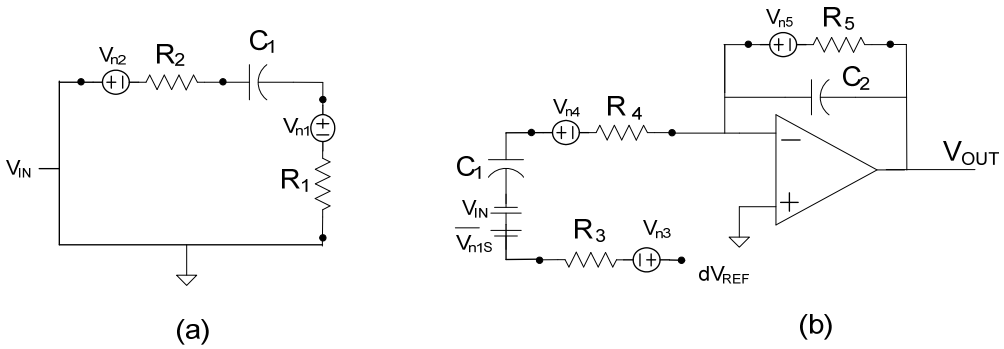


Figure 41. Noise sources in basic gain stage during both clock phases

With a routine analysis during phase Φ_2, we obtain the output voltage expression

$$V_{OUT} = \frac{C_1}{C_2}\left(V_{IN} + dV_{REF} + \vec{V}_{n1}\right) + V_{n4}\frac{C_1}{C_2}\left(\frac{1}{1 + R_4C_1s + \frac{s}{GB}\left(1 + \frac{C_1}{C_2} + R_4C_1s\right)}\right) \qquad (4.40)$$

where the resistor R_4 actually represents the sum of R_3 and R_4. It follows that the RMS output voltage due to R_4 is given by

$$V_{OUTn4\,RMS} = \sqrt{\int_{f=0}^{\infty} S_{R4}\left(\frac{C_1}{C_2}\right)^2 \left|\frac{1}{1 + R_4C_1s + \frac{s}{GB}\left(1 + \frac{C_1}{C_2} + sR_4C_1\right)}\right|^2 df} \qquad (4.41)$$

As before, the critical switch size of R_4 for settling during the phase Φ_2 is approximately given by

$$R_4 = \frac{1}{C_1\beta GB} \qquad (4.42)$$

If we define the parameter θ to characterize how much smaller the resistor is than the critical value, then we can express R_4 as

$$R_4 = \frac{\theta}{C_1\beta GB} \qquad (4.43)$$

substituting into the expression for the output voltage, we obtain

$$V_{OUTn4RMS} = \sqrt{\frac{2kT\theta}{C_1\pi}\left(\frac{1-\beta}{\beta}\right)^2 \int_{\omega=0}^{\infty} \left| \frac{1}{1+\omega^2\left[(1+\theta)^2 - 2\theta\beta\right]+\omega^4(\theta\beta)^2} \right|^2 d\omega} \qquad (4.44)$$

This integral is tedious but from MATLAB, the noise contributions summarized in Table 5 were obtained. This shows the RMS output voltage and the total sampled input-referred RMS noise voltage relative to $\sqrt{kT/C_1}$. Also shown in the Table 5 is the effective value of the input sampling capacitor.

The corresponding input-referred noise voltage, when the output is sampled, is

$$\hat{V}_{IN\text{-}RMS} = \sqrt{\frac{kT}{C_1} + \left(\frac{C_2}{C_1}\right)^2 \hat{V}^2_{OUT\,4\text{-}RMS}} \qquad (4.45)$$

From the foregoing equations, we can get another table for charge distribution structure:

Table 5. Noise contributions of switches during Φ_2

		β		
		1/3	1/5	1/9
θ=1	$V_{4\text{-}5RMS}$	1.414	2.83	5.66
	$V_{IN\text{-}RMS}$	1.22	1.22	1.22
	$\mathbf{C_{INEQ}}$	$0.67C_1$	$0.67C_1$	$0.67C_1$
θ=1/2	$V_{4\text{-}5RMS}$	1.154	2.31	4.62
	$V_{IN\text{-}RMS}$	1.15	1.15	1.15
	$\mathbf{C_{INEQ}}$	$0.75C_1$	$0.75C_1$	$0.75C_1$
θ=1/4	$V_{4\text{-}5RMS}$	0.894	1.79	3.58
	$V_{IN\text{-}RMS}$	1.10	1.10	1.10
	$\mathbf{C_{INEQ}}$	$0.83C_1$	$0.83C_1$	$0.83C_1$
θ=0	$V_{4\text{-}5RMS}$	0	0	0
	$V_{IN\text{-}RMS}$	1	1	1
	$\mathbf{C_{INEQ}}$	C_1	C_1	C_1

Again we will determine the critical switch impedance as a function of the clock speed and the resolution of a data converter. It will be assumed that the time allocated to settling time is half of the clock period, that slewing can be neglected, that the RMS noise voltage can at most ½ LSB with a V_{REF} of 1V, and that all of the sampling noise is determined by the capacitor C_1. With these assumptions, the expressions for R_4, GB and the kT/C noise, the Table 5 is obtained.

For When θ =1, we can calculate

$$\begin{aligned} R_4 &= \frac{1}{C_1 \beta GB}, \\ \sqrt{\frac{kT}{C_1}} &= \frac{1V}{2^{n+1}} \\ GB &= \frac{(n_{ST}+1)2\ln 2}{\beta} f_{CLK} \end{aligned} \tag{4.46}$$

substituting into the expression for R_4, we finally obtain

$$R_4 = \frac{1}{kT 2^{2n_{ST}+2}(n_{ST}+1)2\ln 2 f_{CLK}} \tag{4.47}$$

From Excel, we obtain the critical values of R_4 indicated in the Table 6. Similar as in Table 4, the switches will have impedances much smaller than the critical impedance and consequently the continuous-time noise associated with the switches during the transfer mode will play little role and the overall noise will be dominated by the sample and hold noise. At higher speeds and higher resolutions, the continuous-time noise will dominate the total noise.

4.5 Noise Accumulation of Multiple Stages in ADC

In this section, we will investigate how the continuous and S/H noise propagate and accumulate between stages in a pipeline ADC.

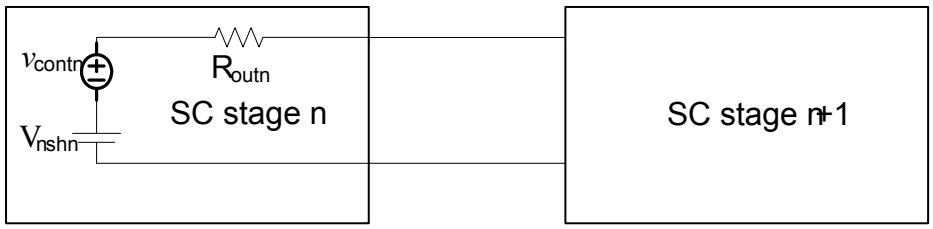


Figure 42. Noise propagating between two stages in an ADC

Table 6. Critical Switch Resistances for Continuous-Time Noise Accumulation

Resolution	Frequency						
	100	1K	10K	100K	1M	10M	100M
8	1.3841e+011	1.3841e+010	1.3841e+009	1.3841e+008	1.3841e+007	1.3841e+006	1.3841e+005
9	3.1142e+010	3.1142e+009	3.1142e+008	3.1142e+007	3.1142e+006	3.1142e+005	31142
10	7.0776e+009	7.0776e+008	7.0776e+007	7.0776e+006	7.0776e+005	70776	7077.6
11	1.622e+009	1.622e+008	1.622e+007	1.622e+006	1.622e+005	16220	1622
12	3.743e+008	3.743e+007	3.743e+006	3.743e+005	37430	3743	374.3
13	8.6891e+007	8.6891e+006	8.6891e+005	86891	8689.1	868.91	86.891
14	2.0274e+007	2.0274e+006	2.0274e+005	20274	2027.4	202.74	20.274
15	4.7518e+006	4.7518e+005	47518	4751.8	475.18	47.518	4.7518
16	1.1181e+006	1.1181e+005	11181	1118.1	111.81	11.181	1.1181
17	2.6399e+005	26399	2639.9	263.99	26.399	2.6399	0.26399
18	62524	6252.4	625.24	62.524	6.2524	0.62524	0.062524
19	14849	1484.9	148.49	14.849	1.4849	0.14849	0.014849
20	3535.6	353.56	35.356	3.5356	0.35356	0.035356	0.0035356

As shown in Figure 42, the output of the n-th stage can be represented by an output resistor R_{outn}, S/H noise as a dc voltage source V_{nshn} and continuous-time noise source V_{contn}. The continuous-time noise is independent of R_{outn}. The continuous-time noise is attributable to the switches and capacitors in the n-th stage. The R_{outn} and v_{contn} come from two total different mechanisms, hence they are independent. The R_{outn} may cause an additional noise

source, but it is ignored in this thesis. In the n+1st stage, the continuous-time noise source is sampled and can be represented by a dc voltage source. So the S/H noise and continuous-time noise can be propagated as a dc voltage source to the output of the n+1st stage and their effects can be calculated separately from the noise of n+1st stage.

4.6 Conclusion

In the foregoing discussion, it was shown that although in all the past literature, only sample and hold noise from the sample phase Φ_1 was considered, the continuous-time noise generated in the hold phase Φ_2 can play an important role in determining the total noise that is present in a SC amplifier. The effects of the noise contributed during phase Φ_2 were shown quantitively in Table 4 and Table 6. For both the flip-around structure and the charge-redistribution structure, if the application requires high frequency or high resolution, the continuous-time noise will not be negligible and may actually become the major contributor to the total noise.

CHAPTER 5 SUMMARY

Switched-capacitor circuits are widely used in today's analog and mixed signal circuits. Although from a circuit design point the field has matured, simplifications in the noise analysis driven by conventional wisdom have resulted in an under-estimation of the actual noise present when those circuits are operated at high speeds. In particular, noise analysis present in the literature includes only the noise generated in the track phase and results in a very simple kT/C noise analysis. However, the continuous-time noise generated in the second phase (or hold phase) has not been included in the total noise.

In this thesis, we have analyzed both the S/H noise and continuous-time noise in terms of power spectral density as well as in terms of a more complete kT/C analysis. Simulation results obtained from Cadence SpectreRF for the PSD analysis were presented as well. The simulation and hand analysis show that the continuous-time noise which is usually ignored in the past can contribute a lot and can even dominate the total noise of the SC gain stage at high frequencies or at high resolution. Evaluations were restricted to the flip-around SC gain stage and the charge-redistribution SC gain stage but similar concerns also exist for other SC amplifier structures.

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